DPB 7000/1

OPERATING AND SERVICE MANUAL

CHAPTER 5 – CARD DESCRIPTIONS

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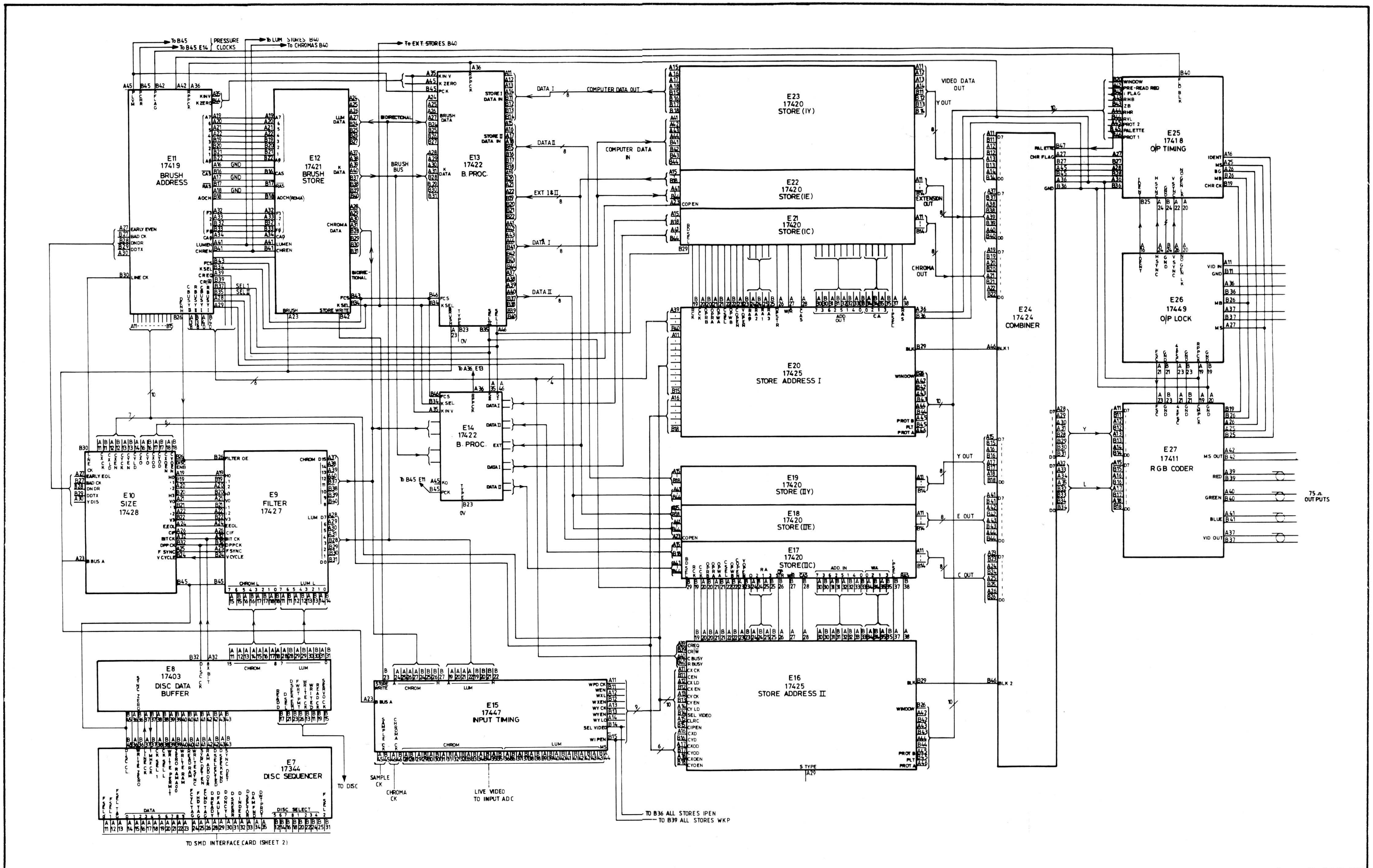

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Figure 1 Paintbox Interconnection Diagram Sheet 1

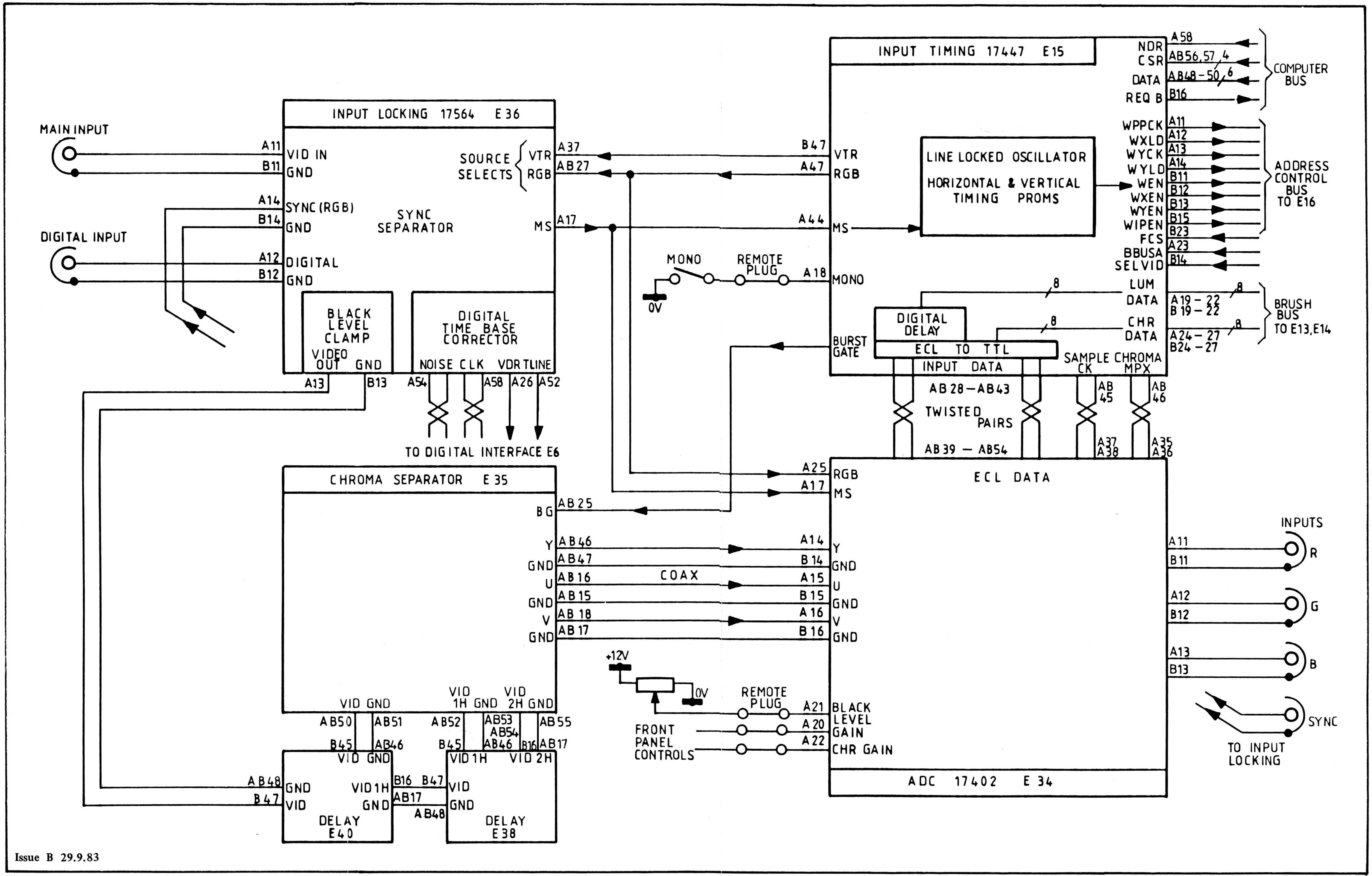

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Figure 1 Paintbox Interconnection Diagram Sheet 2

CHAPTER 5 CARD DESCRIPTIONS

5.1 General

This chapter contains detailed descriptions of the printed circuit cards housed in the DPB 7000/1.

Each description is supported by a circuit diagram, component list and component layout.

COMPUTER CARDS 1 AND 2

17348 AND 17349

1. INTRODUCTION

The DPB 7000/1 Computer comprises two cards, Computer 1 and Computer 2. Computer 1 contains the CPU and its associated support circuitry a serial port for a printer, a parallel output port for driving the DPB 7000/1 control bus and a memory mapped VDU. Computer 2 contains all the RAM and ROM that is required by the Computer and two serial ports.

2. COMPUTER 1

This card uses an MC 68000 16-bit CPU.

2.1 Bus Signals

The address lines from the CPU are latched and buffered in BD, CD and DD. These buffered address lines are used on this card and also go out to the edge connector to feed the Computer 2 card. The CPU data lines are used directly on Computer 1 and are buffered with AC and AD for use with Computer 2.

The 68000 normally works with an asynchronous bus, which means that for any given access cycle, the CPU will wait for a reply back from whatever it is addressing before it allows a data transfer to take place. This reply signal is received at FC15 where it is buffered and fed to DTACK on the CPU. Since the replay signal can come from a variety of places, FC15 and its pull-up resistor form a 'wired OR' point for the various open collector drives feeding back their DTACK signals. FC17 takes a different form of reply signal which will tell the CPU to perform a 6800 type of data transfer. This is another open collector 'wired OR' point. LC monitors the length of all the access cycles output by the CPU. If the CPU does not receive a reply back from a particular location within a given time, LC will continue to count until its QD output goes high which informs the CPU, via its BERR line that a bus time-out has occurred. Shift register LB is used to generate a suitably timed reply signal and its output is buffered by DA and fed to Computer 2 where it is gated to provide a DTACK signal when required.

2.2 Interrupts

FB is an eight input priority encoder which can accept up to seven interrupt lines, these are binary encoded and feed the three interrupt lines on the CPU. The highest level of interrupt is provided by a push button, SW1, mounted on the front of the card. This provides a useful facility during software development. The next level of interrupt comes from the printer serial port, which is also used for system debugging in conjunction with a terminal. Television field pulses appear at REQ A on the edge connector which are then buffered with DA and provide the next level of interrupt via KB. This gate gives the ability to turn off interrupts from this particular source. In a similar way REQB at the edge connector is buffered with EB, gated with KB and fed to the next level of interrupt. REQ B is a signal which, when low, tells the computer that another card in the system (such as the disc controller) has taken control of the DPB 7000/1 control bus. The lowest level of interrupt that is used is generated by either one of the two serial ports on the Computer 2 card and appears as PINT on the edge connector after which it is buffered with FC.

When an interrupt has occured, the CPU will signal that it expects an interrupt vector by putting a high on all three of its function code pins, FC0, FC1 and FC2. This condition is detected by IF which then feeds a signal back to the VPA line on the CPU. This signal informs the CPU that no external interrupt vector will be supplied and that it is to use the appropriate default vector which is held in its program ROM.

The timer, MA, is used to generate a reset signal for the CPU at power on. The CPU can also be reset by pressing SW2 which is mounted on the front of the card. Note that in order to reset the CPU both the HALT and the RESET lines have to be taken low.

2.3 I/O Ports

Address decoding for all the I/O ports is achieved with BC, GB and a few associated gates. GB provides PEN 1 and PEN 2 which are enables for the two serial ports on Computer 2. The other outputs of GB are enables for the I/O ports on Computer 1. GD is a dual output baud rate generator. One output which is fixed at 9600 baud, is fed to Computer 2 via EB for the control boxes' ACIA's. The other output of GD feeds the ACIA FD which is used as the printer port. Its output can be set to any of sixteen different baud rates with SW3.

A sixteen bit output port to the DPB 7000/1 control bus is provided by BA and BB while AA and AB handle data arriving from the control bus. Monostables KA and LA generate strobes NDR TX/RX and DTX which are used to control data transfers to and from the control bus. FA provides a four bit parallel output which also forms part of the DPB 7000/1 control bus. These four lines (CSR0-3) are used to select which card the computer communicates with at any given time.

2.4 VDU

Computer 1 has a built in character display driver, the heart of which is the CRT controller, GA. EA is a 2k x 8 RAM which forms the VDU screen refresh memory; its addresses are normally provided by GA via HB and HA. When the computer needs to update a screen location, HB and HA are tri-stated off, and DC, DB are enabled to pass the appropriate address from the computer to the VDU RAM. IA registers data from the RAM and feeds the character generator, JA. Row addresses for JA come from GA via register IB. Character data from JA is serialised in JB and then combined with the cursor and invert bit in JC. JD blanks the resultant video, LE inverts it, and syncs are added at the base of TR3 which then outputs the VDU video to the edge connector. Syncs generated by the computer card, or those provided by the DPB 7000/1 can be selected by SW4.

CA is a data register which enables the computer to read data from the VDU, while CB is a buffer allowing data from the computer to be written into the RAM. ME is an oscillator running at twice the dot rate of the VDU. This feeds counter KD which addresses ROM KF which provides the various timing signals required by the VDU circuitry via register JF. JE arbitrates between screen refresh and CPU type accesses to the VDU RAM. MF is a phase comparator which locks the VDU horizontal syncs to a reference provided by the DPB 7000/1.

3. COMPUTER 2

This card contains all the RAM and ROM for the computer system and two serial ports for use with the control boxes.

IC14, 28 and 34 are address bus buffers, while IC48 and IC65 are used to buffer the data bus. Additionally IC46 is used to buffer miscellaneous control signals.

3.1 RAM Operation

IC13 is an address comparator for the RAM and gives a low on pin 19 when the address on the most significant bits of the address bus match that set up on the address switch. IC27 contains a refresh counter and a three way multiplexer, which selects row address, column address or its internal refresh address and drives all sixteen RAM chips in parallel. The most significant address line of the RAMs is fed from multiplexer IC25 via buffer IC23.

A RAM access cycle is started when an appropriate address match is detected with IC13 pin 19 going low. If a refresh cycle is not in progress, pin 2 of IC24 will be low and a low will appear on IC24 pin 3. After being gated by the data strobe signal and buffered by IC61 the negative going edge will propagate down the delay line IC44. This signal also clocks IC45 which tells the refresh circuit that the RAM is busy. Pin 13 of the delay line outputs a RAS signal (Row Address Strobe) which is buffered by IC23, combined with refresh RAS in IC49 and further buffered by two more sections of IC23 which then drive the two rows of eight RAMs. Pin 12 of IC44 is buffered by IC61 and drives the multiplexer input of IC27 which then switches from row address to column addresses. Pin 5 of IC44 is buffered by IC23 and is gated by two sections of IC24. This provides a means of individually selecting the high byte, low byte or both bytes corresponding to a location in the RAM. After being buffered in IC23 these signals drive the CAS (Column Address Strobe) lines of the two rows of eight RAMs. When the negative edge gets close to the end of the delay line, the output of IC32 pulses low which clears the 'RAM busy' register IC45. On reaching the end of the delay line it sends out a low on DTACK via IC31 signalling to the processor that the RAM is ready for a data transfer.

The RFSH CK signal from Computer 1 is divided by sixteen in IC62 to provide refresh requests. A request will clock IC51 pin 8 low which in turn will clear the other half of IC51, putting a high on pin 6. If IC45 pin 6 is not signalling that a RAM access cycle is under way, IC32 will let through a negative edge via IC61 to delay line IC9. This signal also feeds the refresh address enable pin on IC27 via IC43 and sets a high on IC45 pin 8 to signal that a refresh cycle is under way. After a short delay the negative edge appears on pin 3 where it is then buffered by IC23. This signal then clears the refresh request that was being held in IC51 and generates a RAS signal via IC49. When the negative edge reaches the end of IC9 it presets IC51 which, through IC32, sends a positive edge down IC9. This returns RAS to a high level and on reaching the end of IC9 clocks IC45 signalling the end of a refresh cycle. IC29 and IC50 buffer the output data from the RAM.

3.2 ROM

Address decoding for the ROM is provided by IC11, when an address match is found pin 19 of IC11 goes low, enabling decoder IC60 which selects one of the eight pairs of ROMs. The output from IC11 also feeds IC32 where it is inverted and then gated by TRPLY from Computer 1 in IC49. This generates a DTACK signal corresponding to ROM accesses. IC26 is a header, the linking of which can be changed to support various sizes of ROM from 16k up to 128k.

3.3 I/O Ports

IC63 and IC64 are serial interfaces used to communicate, IC33 and IC47 are RS422 drivers and receivers.

CAPACITORS

REF.	DESCRIPTION	STOCK CODE
C1-C3	100000pF, 100V, +80%-20%	03/06/0217
C4	470000pF, 35V, 20%	03/03/0032
C5	S.O.T.	
C6	100000pF, 100V, +80%-20%	03/06/0217
C7	10000pF, 100V, +80%-20%	03/06/0101
C8	2.2µF, 35V, 20%	03/03/0059
C9	100000pF, 100V, +80%-20%	03/06/0217
C10	390pF, 100V, 20%	03/06/0632
C11-C13	150pF, 100V, 20%	03/06/0365
C14-C16	10µF, 25V, 20%	03/03/018Y
C17, C18	10µF, 25V, 20%	03/03/018Y
C19	100000pF, 100V, +80%-20%	03/96/0217
C20-C28	NOT FITTED	
C29-C45	100000pF, 100V, +80%-20%	03/06/0217
C46-C55	NOT FITTED	
C56	680pF, 100V, 10%	03/06/0063
C57	10000pF, 100V, +80%-20%	03/06/0101

RESISTORS

R1, R2	470Ω, 2%, 100ppm	01/01/0557
R3	NOT FITTED	
R4, R5	2.2kΩ, 2%, 100ppm	01/01/0727
R6, R7	10kΩ, 2%, 100ppm	01/01/0948
R8	4.7kΩ, 2%, 100ppm	01/01/084Y
R9	1.8kΩ, 2%, 100ppm	01/01/070Y
R10, R11	1M, 5%, 250ppm	01/01/1332
R12	470Ω, 2%, 100ppm	01/01/0557
R13, R14	10kΩ, 2%, 100ppm	01/01/0948
R15	4.7kΩ, 2%, 100ppm	01/01/084Y
R16-R19	10kΩ, 2%, 100ppm	01/01/0948
R20	330Ω, 2%, 100ppm	01/01/1723
R21	150Ω, 2%, 100ppm	01/01/0387
R22	22Ω, 2%, 100ppm	01/01/0131
R23	300Ω, 2%, 100ppm	01/01/0506
R24	220Ω, 2%, 100ppm	01/01/0441
R25	75Ω, 2%, 100ppm	01/01/0263
R26-R29	10kΩ, 2%, 100ppm	01/01/0948
R30	4.7kΩ, 2%, 100ppm	01/01/084Y
R31	10kΩ, 2%, 100ppm	01/01/0948
R32	220Ω, 2%, 100ppm	01/01/0441
R33	2.7kΩ, 2%, 100ppm	01/01/0743
R34	47kΩ, 2%, 100ppm	01/01/1103
R35	10kΩ, 2%, 100ppm	01/01/0948
R36	12kΩ, 2%, 100ppm	01/01/0964
R37	220Ω, 2%, 100ppm	01/01/0948
R38	470Ω x 10, 125mW, 5%, 300ppm	01/08/164Y
R39	10kΩ x 4, 125mW, 5%, 300ppm	01/08/1128
R40	51kΩ, 250mW, 2%, 100ppm	01/01/1111

SEMICONDUCTORS

D1	Diode	06/01/0067
D2	Diode	06/05/0018

SEMICONDUCTORS (Cont.)

REF.	DESCRIPTION	STOCK CODE
TR1	Transistor PNP TO92	05/01/0276
TR2	Transistor NPN TO92	05/01/0268
TR3	Transistor NPN TO18	05/01/2909

INTEGRATED CIRCUITS

AA, AB	74LS244	04/01/2828
AC, AD	74LS245	04/01/3824
BA, BB	74LS374	04/01/3328
BC	74S133	04/01/3638
BD	74LS373	04/01/3956
CA	74LS374	04/01/3328
CB	74LS244	04/01/2828
CD	74LS373	04/01/3956
DA-DC	74LS244	04/01/2828
DD	74LS373	04/01/3956
EA	HM6116P3	04/03/345Y
EB	74LS244	04/01/2828
EC	MC68000L	04/03/3507
FA	29LS18	
FB	74LS148	04/01/3662
FC	74LS244	04/01/2828
FD	MC6850	04/03/1687
GA	SY6545	04/03/2799
GB	74LS138	04/01/109Y
GC	74LS244	04/01/2828
GD		28/02/035X
HA	74LS173	04/01/2836
HB	74LS373	04/01/3956
HC, HD	74LS32	04/01/3506
HE	74LS04	04/01/0191
IA	74LS273	04/01/3115
IB, IC	74LS174	04/01/1422
ID	74LS04	04/01/0191
IE	74LS32	04/01/3506
IF	74LS10	04/01/3123
JA	74S262	04/01/622X
JB	74LS166	04/01/319Y
JC	74LS86	04/01/0833
JD	74LS10	04/01/3123
JE	74LS74	04/01/0728
JF	74S175	04/01/1449
KA	74LS221	04/01/1589
KB, KC	74LS00	04/01/006X
KD	74S163	04/01/370Y
KE	7417	04/01/0361
KF	82S123	04/01/2313
LA	74LS221	04/01/1589
LB	74LS164	04/01/3719
LC	74LS161	04/01/1287
LD	74LS32	04/01/3506
LE	74LS04	04/01/0191
MA		04/01/2224
MB	29LS18	
MC	74LS163	04/01/1317
MD		28/02/021X
ME		28/02/0333
MF		04/03/0079

MISCELLANEOUS

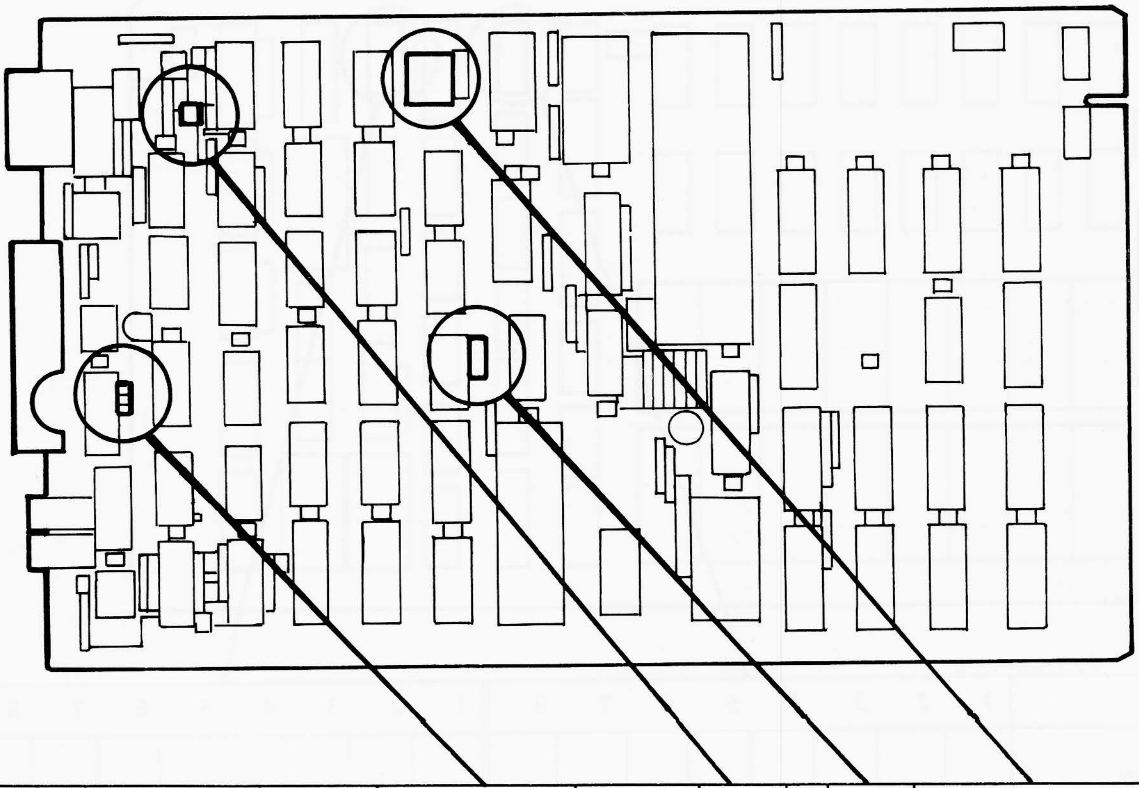
SW1, SW2	Switches	26/04/0442
SW3	Switch	26/06/0176
SW4, SW5	Switches	26/06/029X

17348 Component List

REF.	DESCRIPTION	STOCK CODE
CAPACITORS		
C1	10μF, 25V, 20%	03/03/018Y
C2, C3	1μF, 35V, 20%	03/03/004Y
C4-C64	100000pF, 50V	03/06/0233
C65-C70	270pF, 100V	03/06/0349
RESISTORS		
R1, R2	220Ω x 8, 125mW	01/08/1039
R3	220Ω x 7, 125mW	01/08/1705
R4	10kΩ x 7, 125mW	01/08/1713
R5-R8	NOT FITTED	
R9, R10	3.3kΩ, 125mW	01/02/042Y
R11-R17	47Ω, 125mW	01/02/0099
R18, R19	100Ω, 125mW	01/02/0153
R20	10kΩ x 7, 125mW	01/08/1713
R21-R24	1kΩ, 125mW	01/02/0331
R25	220Ω x 7, 125mW	01/08/1705
R26	47Ω, 125mW	01/02/0099
INTEGRATED CIRCUITS		
IC1-IC8	HM4864	04/03/3353
IC9		30/01/028Y
IC10	435166-1	26/05/0073
IC11	25LS2521	04/01/4391
IC13	435166-1	26/05/0073

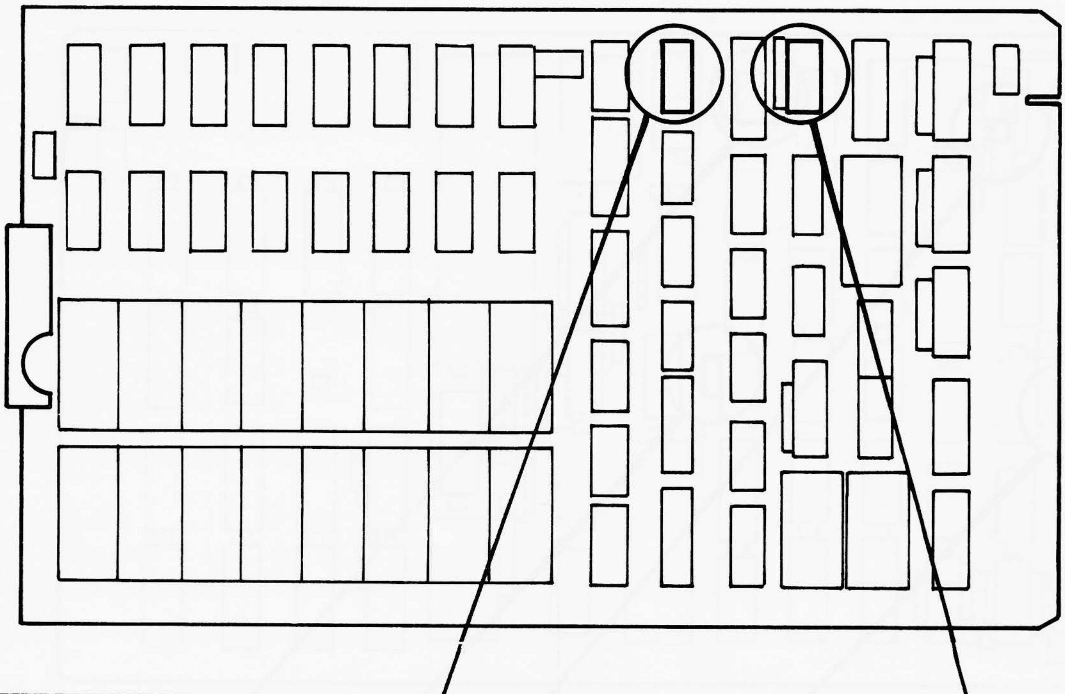
REF.	DESCRIPTION	STOCK CODE
INTEGRATED CIRCUITS (Cont.)		
IC14	74LS244	04/01/2828
IC15-IC22	HM4864	04/03/3353
IC23	74LS244	04/01/2828
IC24	74LS32	04/01/3506
IC25	74LS158	04/01/3689
IC26	70616-11	08/07/0016
IC27	3242	04/03/1709
IC28, IC29	74LS244	04/01/2828
IC30	74LS21	04/01/345X
IC31	7405	04/01/0205
IC32	74LS00	04/01/006X
IC33	AM26LS31	
IC34	74LS244	04/01/2828
IC35-IC42	C932802	08/07/0229
IC43	74LS04	04/01/0191
IC45	74LS74	04/01/0728
IC46	74LS244	04/01/2828
IC47	AM26LS32	04/01/4413
IC48	74LS245	04/01/3824
IC49	74LS08	04/01/417Y
IC50	74LS244	04/01/2828
IC51	74LS74	04/01/0728
IC52-IC59	C932802	08/07/0229
IC60	74LS138	04/01/109Y
IC61	74LS244	04/01/2828
IC62	74LS163	04/01/1317
IC63, IC64	6850	04/03/1687
IC65	74LS245	04/01/3824

17349 Component List



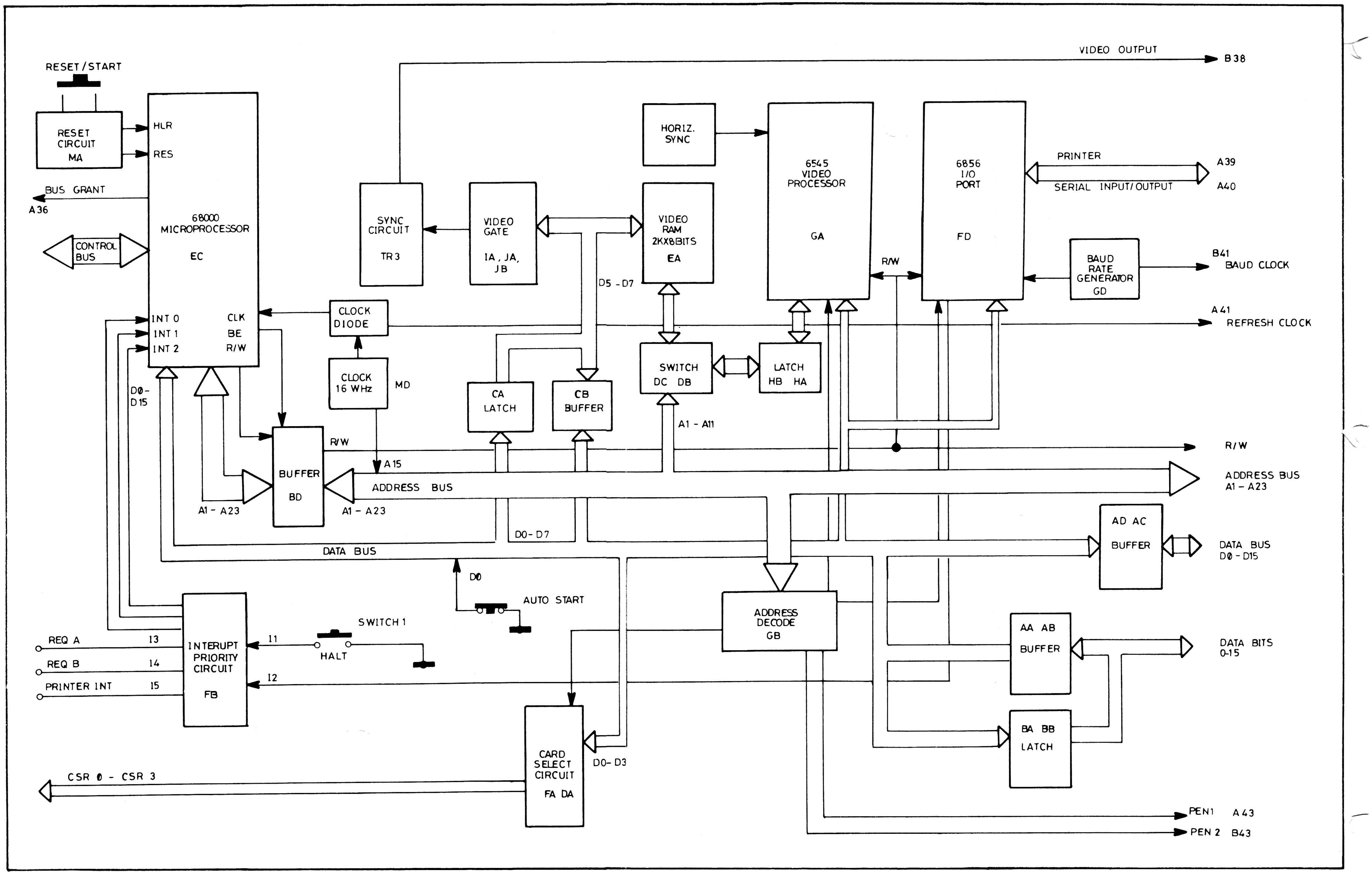
	LINKS W6	W7	W8		SW 5		SW 4	1	2	3	4
BAUD RATE 19200								OFF	OFF	OFF	OFF
9600								ON	OFF	OFF	OFF
7200								OFF	ON	OFF	OFF
4800								ON	ON	OFF	OFF
3600								OFF	OFF	ON	OFF
2400								ON	OFF	ON	OFF
2000								OFF	ON	ON	OFF
1800								ON	ON	ON	OFF
1200								OFF	OFF	OFF	ON
600								ON	OFF	OFF	ON
300								OFF	ON	OFF	ON
START UP IN MONITOR					UP						
DATA DISPLAY SYNCS INIT							DWN				
DATA DISPLAY SYNCS EXT							UP				
XTAL OSC 8MHz		x	x								
XTAL OSC 4MHz	x		x								
NORMAL PAINTBOX CONFIGURATION		x	x		DWN		DWN	ON	OFF	OFF	OFF

Figure 1 17348 Computer 1 Card Switch Configurations

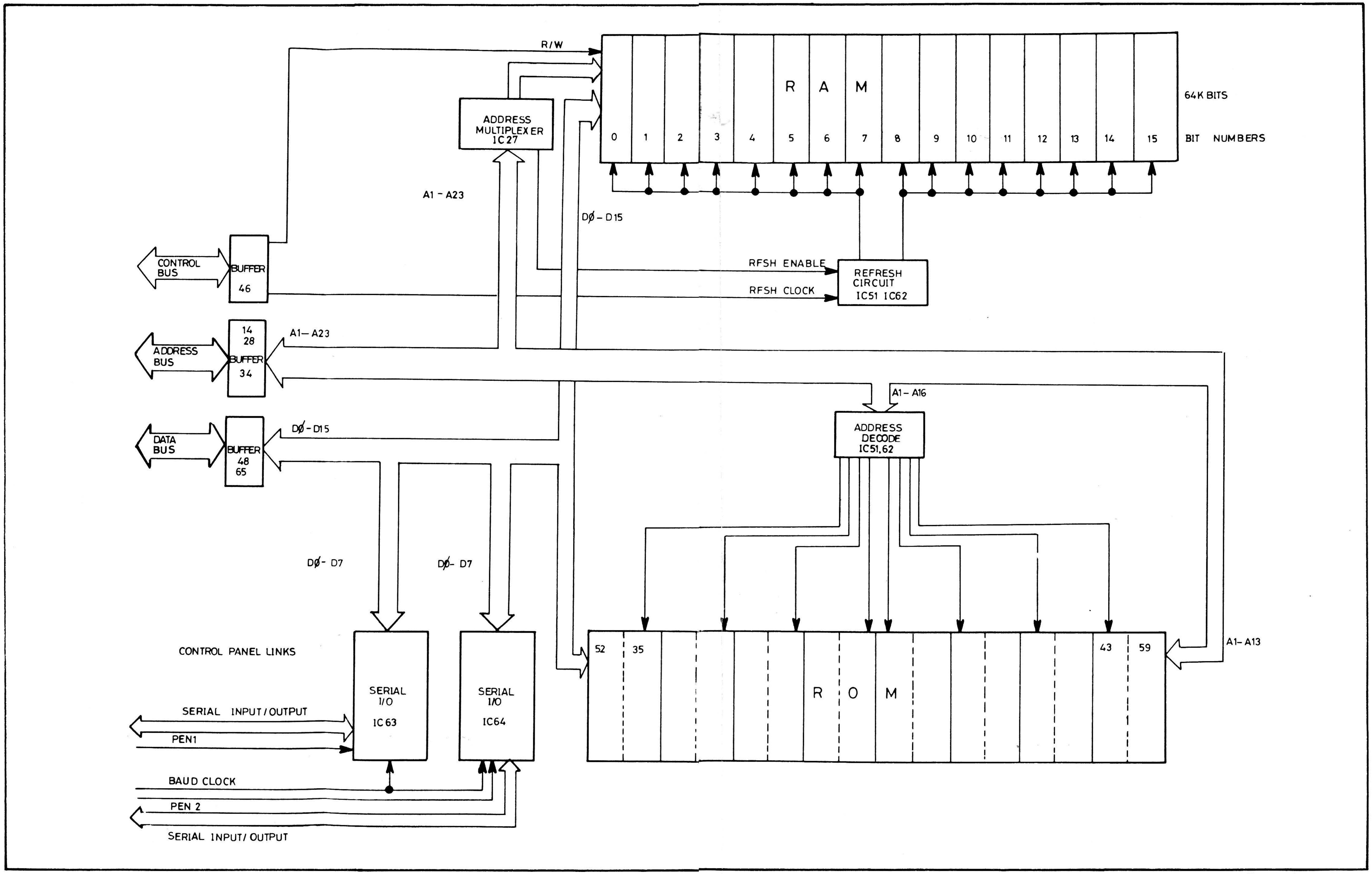


	1	2	3	4	5	6	7	8	1	2	3	4	5	6	7	8
STANDARD CONFIGURATION																
V2 & V2A	ON	ON	ON	ON	ON	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF
V1.6	ON	ON	ON	ON	ON	ON	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF
V3.1 V3A	ON	ON	ON	ON	ON	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
STANDARD CONFIGURATION																
V3	ON	ON	ON	ON	ON	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF

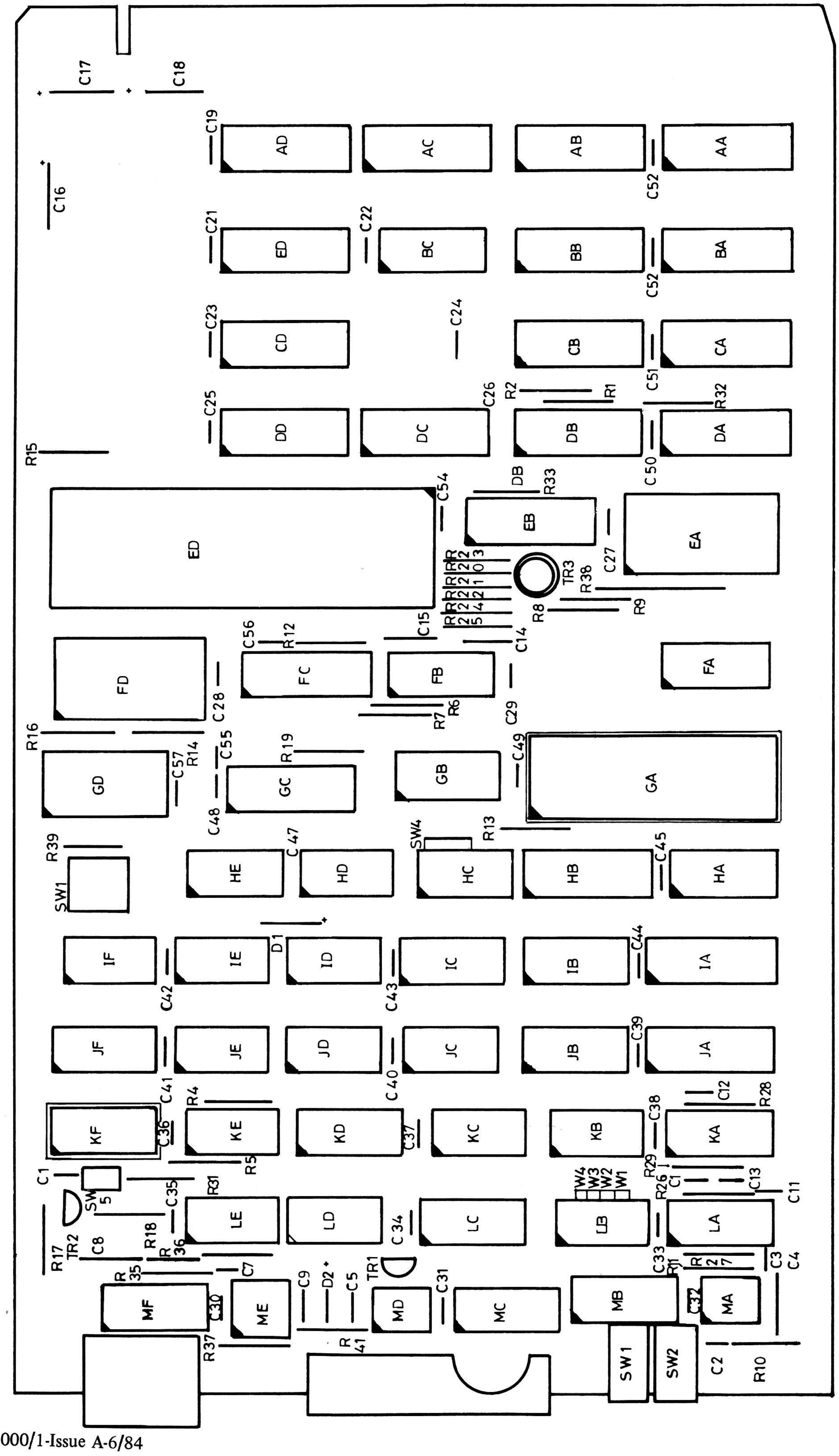
Figure 2 17349 Computer 2 Card Switch Configurations

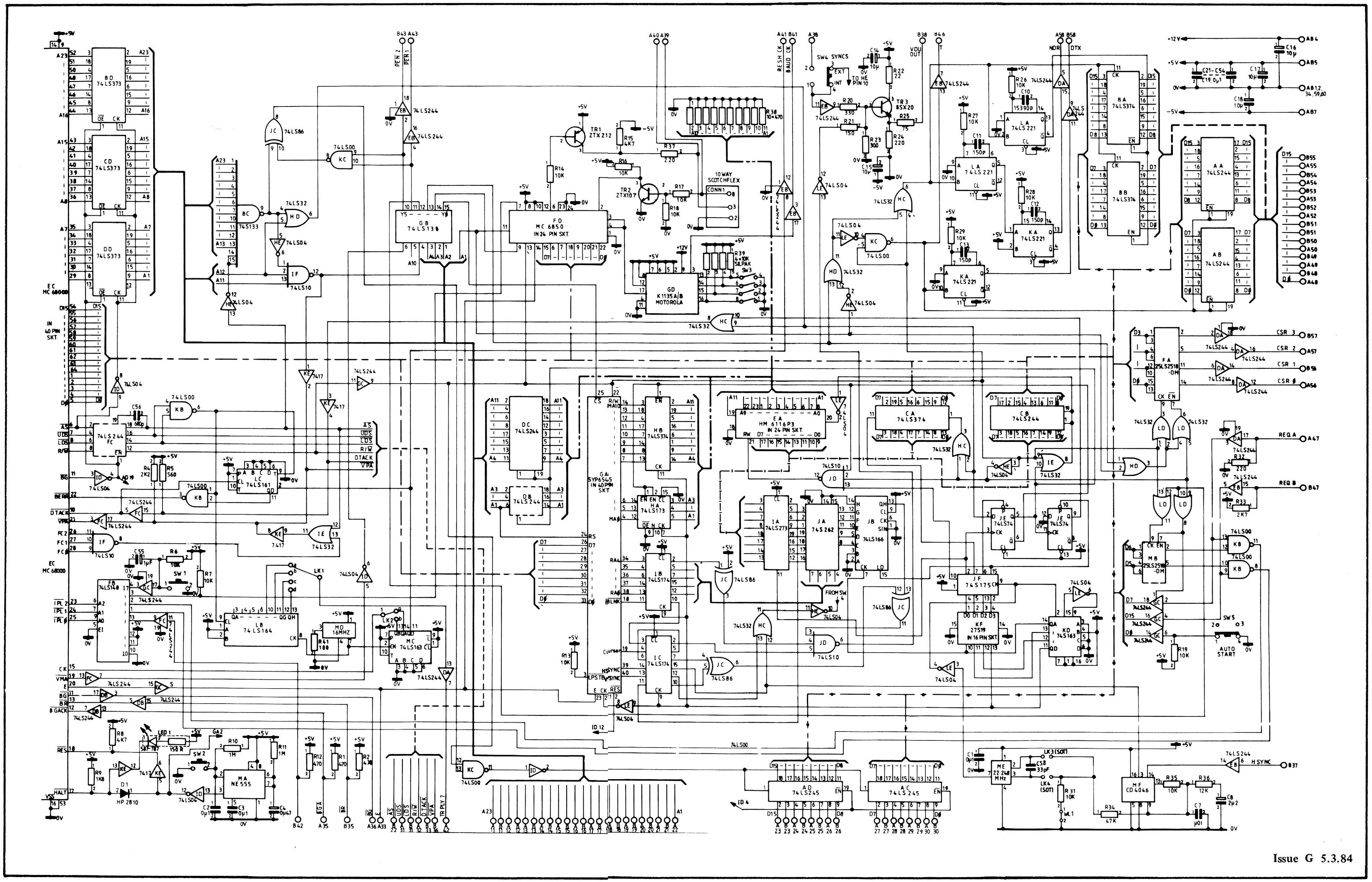


17348, Figure 3 Computer 1 Card Block Diagram

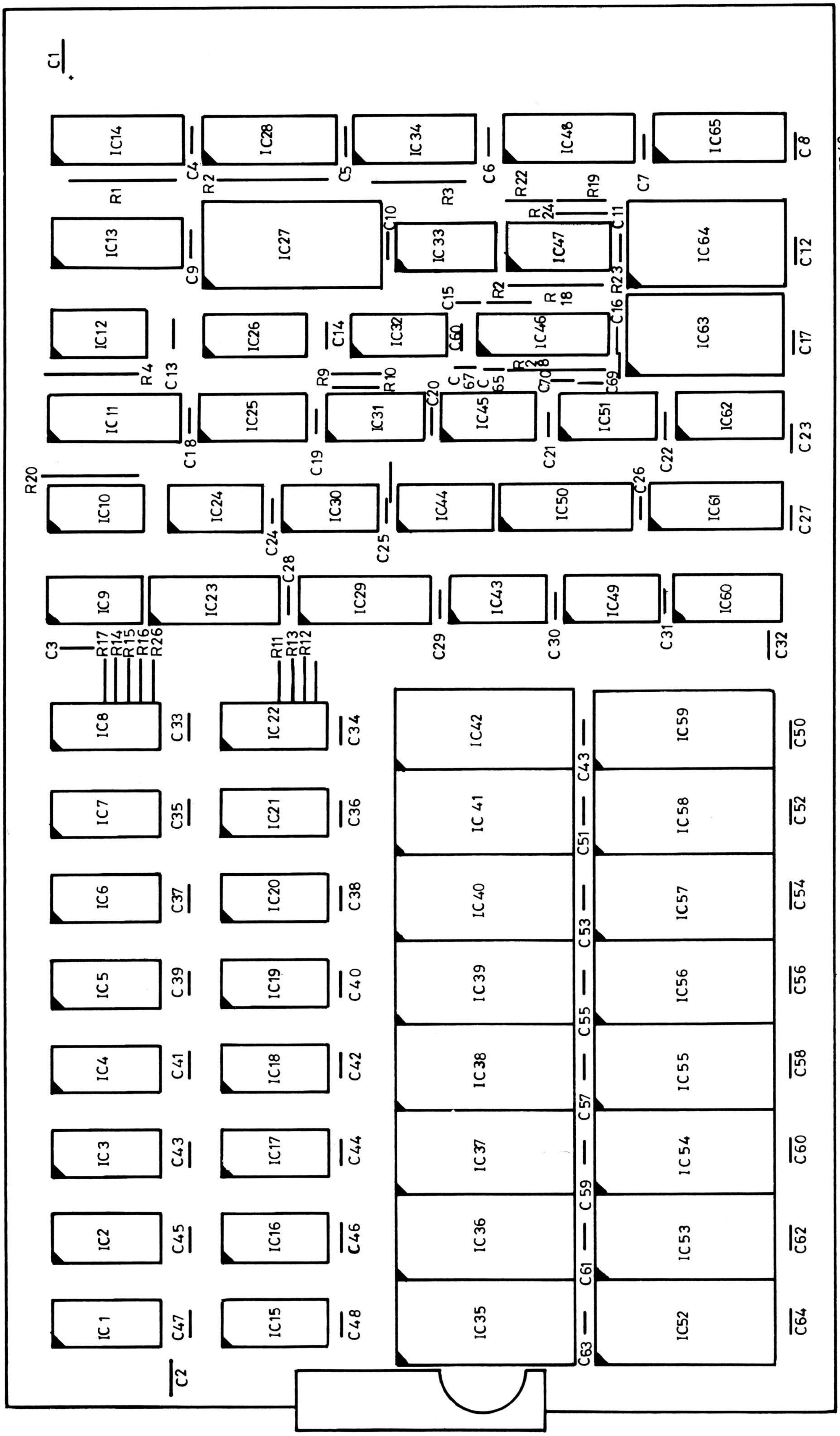


17349, Figure 4 Computer 2 Card Block Diagram


C17
C18
C19
AD
AC
AB
AA
17348
C16
C52
C21
ED
C22
BC
BB
BA
C52
C23
CD
C24
CB
CA
R2
R1
C51
R32
C25
DD
DC
C26
DB
DA
C50
R15
C54
DB
R33
ED
EB
EA
C27
R20
R21
R22
R23
R24
R25
TR3
R38
R8
R9
C14
C15
C56
R12
FC
FB
FA
FD
C28
R6
R7
C29
R16
R14
C55
C57
R19
GD
GC
GB
C49
GA
R13
C48
C47
SW4
R39
SW1
HE
HD
HC
HB
C45
HA
D1
IF
IE
ID
IC
IB
C44
IA
C42
C43
JF
JE
JD
JC
JB
C39
JA
C41
R4
C40
C12
R28
KF
C36
KE
KD
C37
KC
KB
C38
KA
R5
C1
SW5
R31
C35
R29
R26
C1
C13
C11
W4
W3
W2
W1
LE
LD
C34
LC
LB
LA
R17
TR2
C8
R18
R36
C33
R11
R27
C3
C4
R35
C7
C9
D2
C5
TR1
C31
MF
C30
ME
MD
MC
MB
C32
MA
R37
R41
SW1
SW2
C2
R10



17348, Figure 5 Computer 1 Card : Circuit Diagram and Component Layout


C1
IC14
C4
IC28
C5
IC34
C6
IC48
IC65
C8
17349
R1
R2
R3
R22
R19
C7
R24
C10
C11
IC13
C9
IC27
IC33
IC47
IC64
C12
C15
R21
R18
R23
C16
IC12
IC26
C14
IC32
C60
IC46
IC63
C17
R4
C13
R9
R10
C67
C65
R28
C70
C69
IC11
C18
IC25
C19
IC31
C20
IC45
C21
IC51
C22
IC62
C23
R20
IC10
IC24
C24
IC30
C25
IC44
IC50
C26
IC61
C27
IC9
IC23
C28
IC29
C29
IC43
C30
IC49
C31
IC60
C32
C3
R17
R14
R15
R16
R26
R11
R13
R12
IC8
C33
IC22
C34
IC42
C43
IC59
C50
IC7
C35
IC21
C36
IC41
C51
IC58
C52
IC6
C37
IC20
C38
IC40
C53
IC57
C54
IC5
C39
IC19
C40
IC39
C55
IC56
C56
IC4
C41
IC18
C42
IC38
C57
IC55
C58
IC3
C43
IC17
C44
IC37
C59
IC54
C60
IC2
C45
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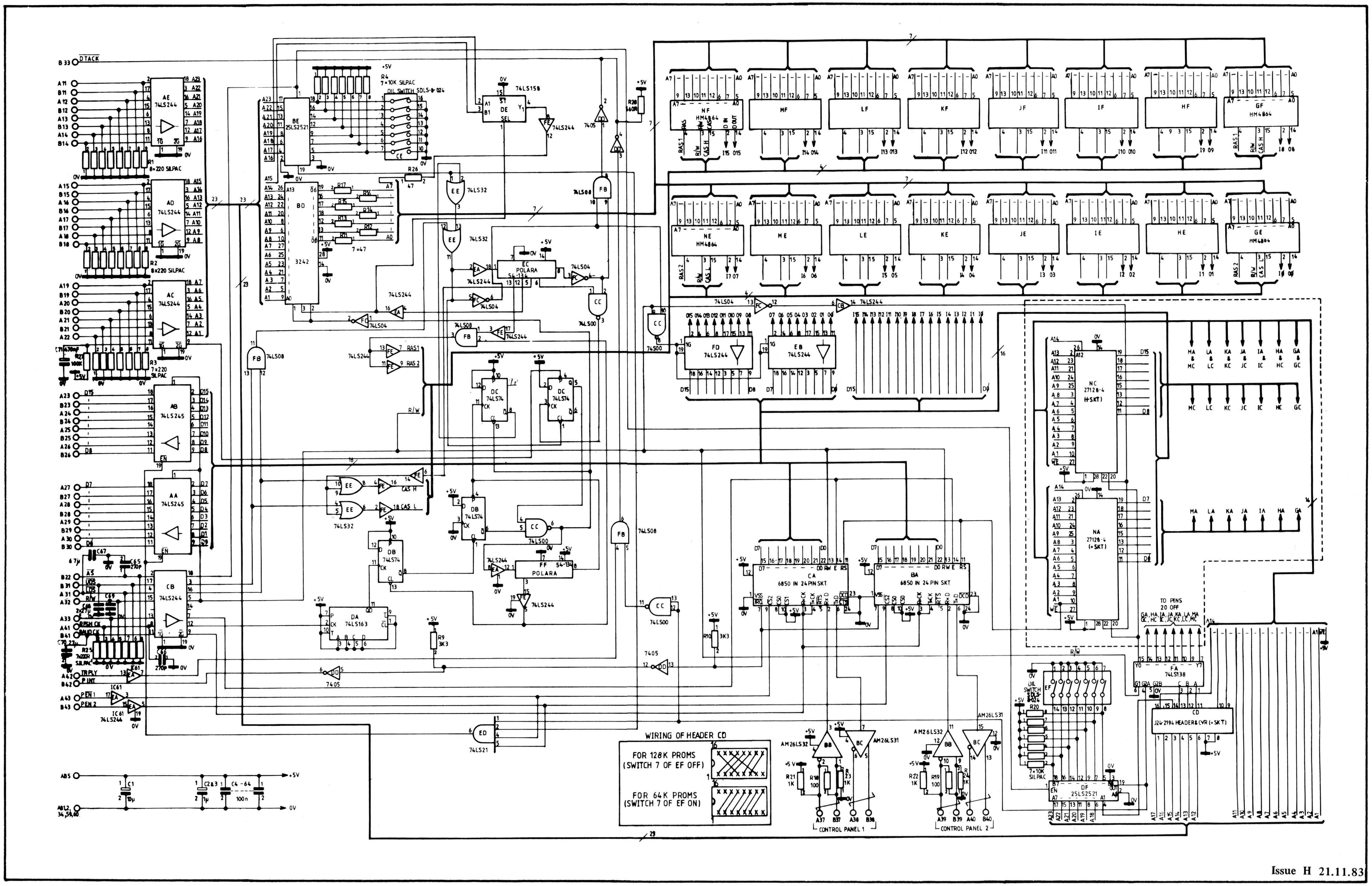
C63
IC52
C64
C2



17349, Figure 6 Computer 2 Card : Circuit Diagram and Component Layout

DISC SEQUENCER CARD

17344F AND 17704B

1. INTRODUCTION

This card converts the disc data transfer commands from the Paintbox computer system into control data used by the discs. The card also handles the status data from the discs which is used by the computer system for checking data transfers.

2. CIRCUIT DESCRIPTION

This card uses an AM 2910 bit slice sequencing element. This provides the addressing for a 56-bit wide micro code word which is stored in seven 28L22 PROMs. The output from the PROMs is registered before use, providing signals S0 through S55.

S0 through S7 are fed back to the 2910 and are used to supply any jump address which may be required by a sequencer instruction. S8 through S11 are also fed back to the 2910 and constitute a 4-bit instruction to the sequencer. The gate GH, which is in series with the sequencer instruction word, gives the ability to force the instruction code to zero which is the 'jump to start' code. The sequencer is forced to 'start' state by any of the following.

(a) Absence of 1MHz clock, causing monostable DB to time out and clear the two halves of BG.

(b) A "panic" clearcommand issued by the control computer, usually invoked by a time out condition occurring due to a sequencer hang caused by a disc error. The control computer issues a "panic" clear by setting the CSR code to fifteen and putting TX/RX low. This is detected by CA which clears BG.

(c) An end of a sequencer program signalled by setting S25 which clears the first half of BG, which clears the second half on the next clock cycle.

S12 through S16 drives FF, FE, FD, FC and FB which form a 1 of 32 data selector. This provides 32 condition code inputs to the AM2910.

S17 and S18 are CLOCK and CLEAR to EF and EE. These are used to count lines, a count of 25 being detected by bit 0 of DF which is fed to the sequencer as a condition code. Bit 1 of DF is unused.

S19 and S20 are CLOCK and CLEAR to ED. Only the Qa output is used at the moment to flag on error condition to the control computer.

S21 and S22 are CLOCK and CLEAR to EC. An Auto-head mode EC selects head numbers, with PROM DC acting as a comparator. At present this mode is not invoked and DC is replaced with a link between pins 5 and 12 of the PROM socket.

S23, S35, S36 and S37 are four signals used to strobe the appropriate information onto the disc bus cable.

S24 enables the cylinder number data onto the disc bus cable.

S27 enables the command word to the disc onto the bus cable, S26 through S34 being the actual command word.

S40 through S47 and S53 are control signals to the Disc Data Buffer cards and are explained in that cards description.

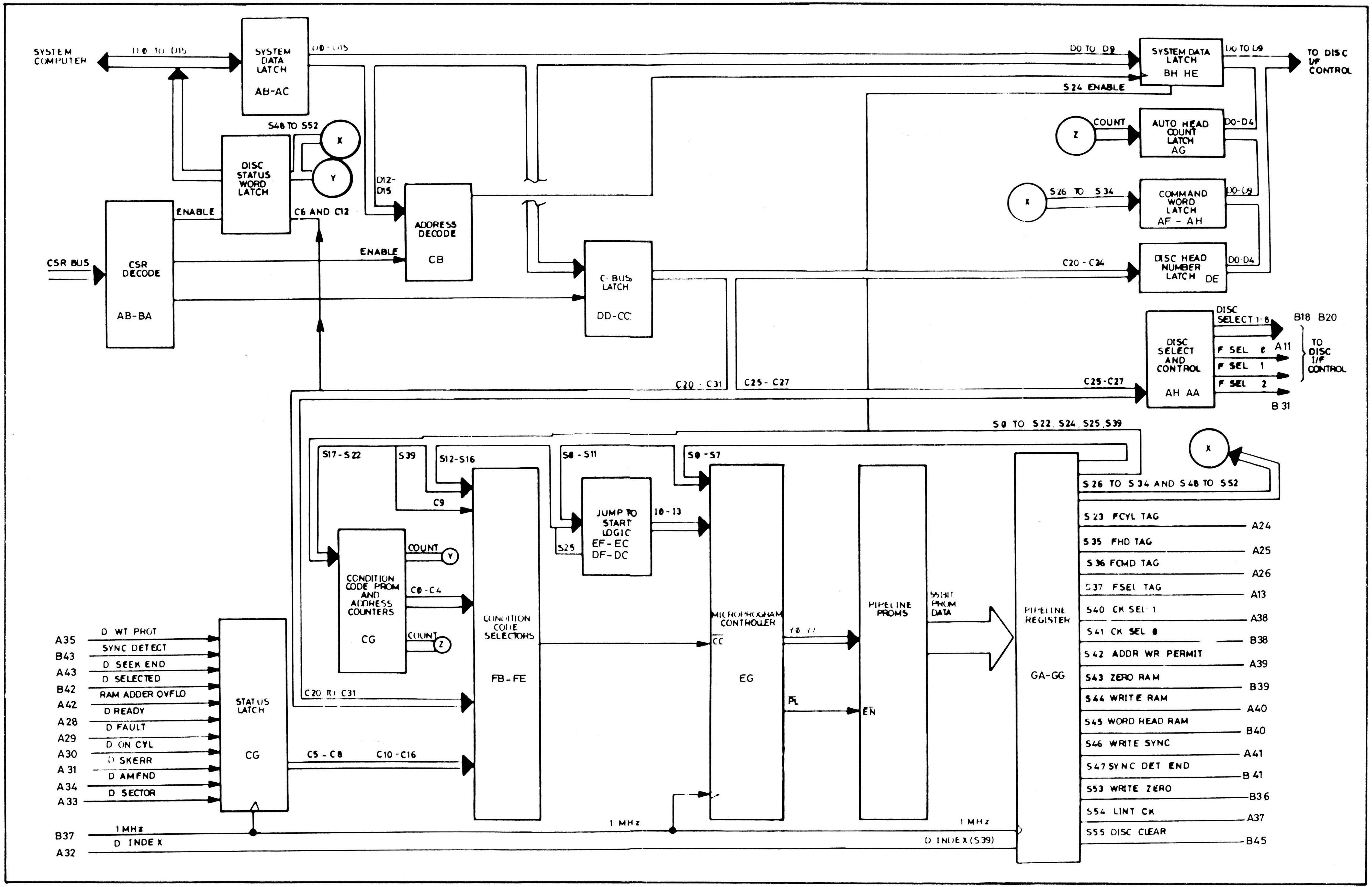
S54 is a disc-rate line sync output and S55 a disc field reset.

AA, AB and AC buffer the control bus. BA detects CSR code = 1 indicating a disc access is required. CB decodes the top 4-bits of the control word. If the value of these bits is 0, the data on the first ten lines of the control bus is interpreted as a cylinder number and is clocked into AE and BH. If the value of the top four bits is two, the data and the other twelve lines of the control bus are interpreted as a command to the disc sequencer and are clocked into DD and CC. Additionally BG pin 6 is clocked to a zero pulling REQB low, signalling a "bus busy" state. This remains low until an end of command is flagged by the sequencer which clears BG. BC holds the disc status word which can be read by the control computer.

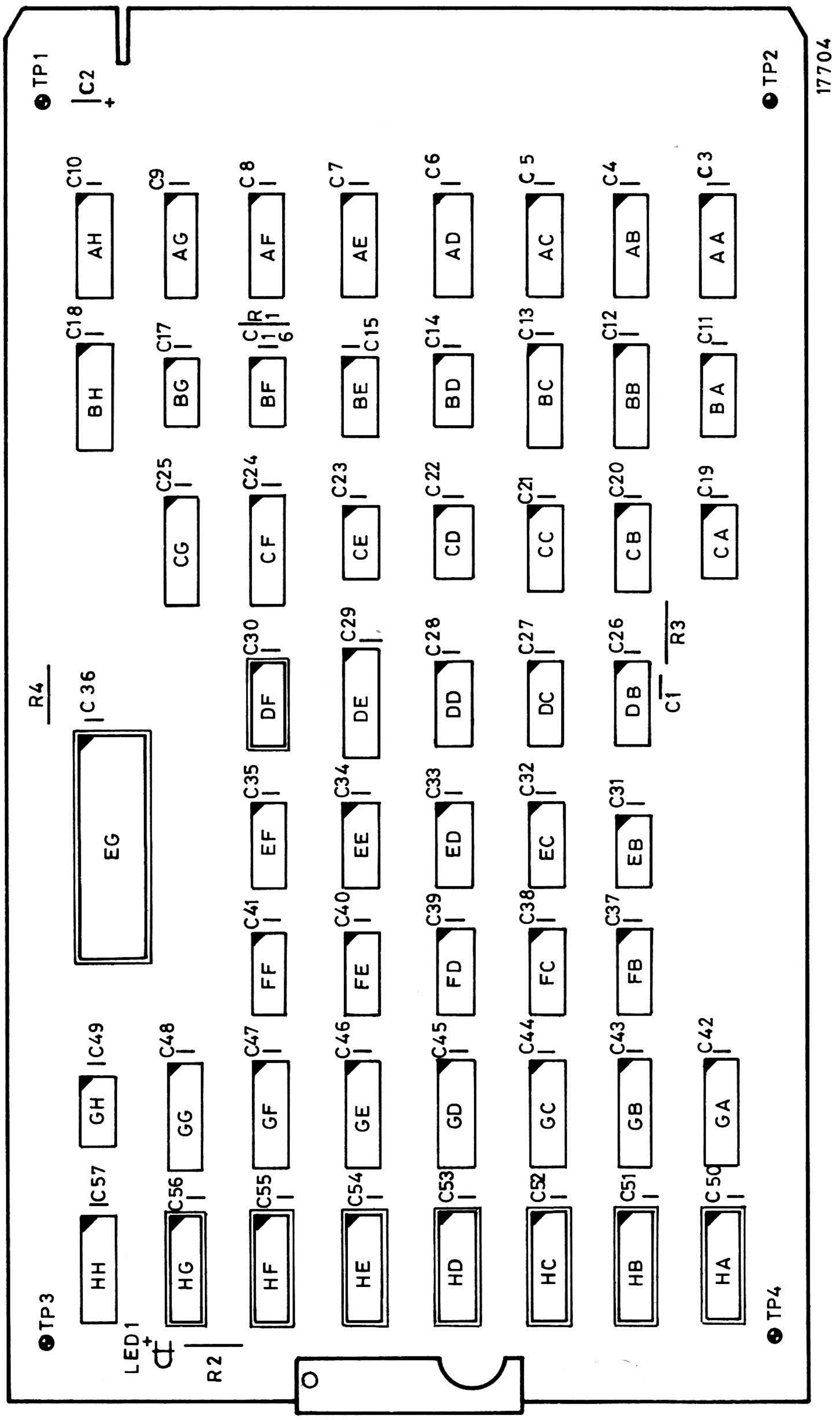
Bits 0 through 3 of the command word hold the disc head number and with bit 4 low, the head number is tri-stated onto the disc bus with DE. Bits 5, 6 and 7 of the command word hold the drive number. 5 and 6 are a 1 of 4 select to the disc bus cable. BE decodes all three drive number lines and feeds the SMD Interface cards.

REF	DESCRIPTION	STOCK CODE
CAPACITORS		
C1	33000pF, 100V, 10%	03/06/087X
C2	22μF, 16V, 20%	03/03/0253
C3-C57	100000pF, 50V, +80% −20%	03/06/0233
RESISTORS		
R1	4.7kΩ, 250mW, 2%, 100ppm	01/01/084Y
R2	470Ω, 250mW, 2%, 100ppm	01/01/0557
R3	22kΩ, 250mW, 2%, 100ppm	01/01/1014
R4	1kΩ, 250mW, 2%, 100ppm	01/01/0646
INTEGRATED CIRCUITS		
AA-AC	74LS244N	04/01/2828
AD	74LS240N	04/01/2879
AE	74LS534J	04/01/5126
AF-AH	74LS240N	04/01/2879
BA	74LS138N	04/01/109Y
BB	74LS244N	04/01/2828
BC	74LS374N	04/01/3328
BD	74LS04N	04/01/0191
BE	74LS138N	04/01/109Y
BF	74LS09N	04/01/1333
BG	74LS74N	04/01/0728
CA	74LS30N	04/01/0469
CB	74LS138N	04/01/109Y
CC	74LS174N	04/01/1422
CD	74LS08N	04/01/417Y
CE	74LS32N	04/01/3506
CF	74LS240N	04/01/2879
DB	74LS123N	04/01/1015
DC	PROGRAMMED SET MAKE FROM THE FOLLOWING (REF ONLY) 1 X 04/01/2305 (7611A-5) 1 X 04/01/2313 (74S288) 7 X 04/01/3107 (6309-1)	
DD	74LS174N	04/01/1422
DE	74LS240N	04/01/2879
DF	PROGRAMMED SET MAKE FROM THE FOLLOWING (REF ONLY) 1 X 04/01/2305 (7611A-5) 1 X 04/01/2313 (74S288) 7X 04/01/3107 (6309-1)	
EB	74LS04N	04/01/0191
EC-EF	74LS161N	04/01/1287
EG	2910PC	04/01/8389
FB-FE	74LS251N	04/01/384Y
FF	74LS139N	04/01/3646
GA-GG	74LS374N	04/01/3328
HA-HG	PROGRAMMED SET MAKE FROM THE FOLLOWING (REF ONLY) 1 X 04/01/2305 (7611A-5) 1 X 04/01/2313 (74S288)	
HH	74LS244N	04/01/2828

17344 Component List



17344, Figure 1 Disc Sequencer Card Block Diagram


17704
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TP2
TP3
TP4
C2
AA
AB
AC
AD
AE
AF
AG
AH
BA
BB
BC
BD
BE
BF
BG
BH
CA
CB
CC
CD
CE
CF
CG
DB
DC
DD
DE
DF
EB
EC
ED
EE
EF
EG
FB
FC
FD
FE
FF
GA
GB
GC
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GE
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HA
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HG
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C1
C3
C4
C5
C6
C7
C8
C9
C10
C11
C12
C13
C14
C15
C16
C17
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C39
C40
C41
C42
C43
C44
C45
C46
C47
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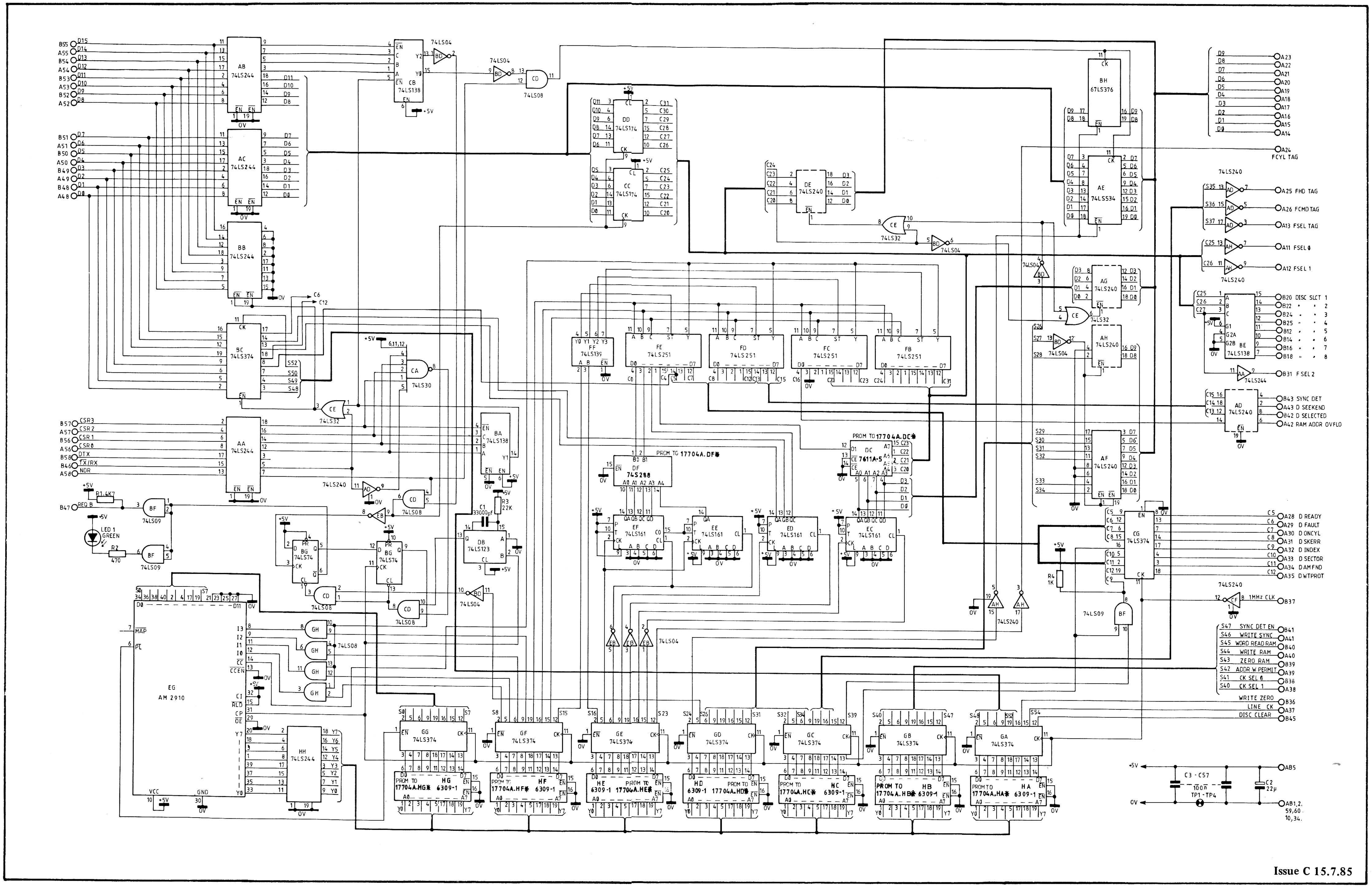
R1
R2
R3
R4
LED1



Issue C 15.7.85

17344/17704, Figure 2 Disc Sequencer Card : Circuit Diagram and Component Layout

DISC DATA BUFFER CARD

17703

1. INTRODUCTION

This card provides parallel to serial conversion for writing to the disc, serial to parallel conversion for reading from the disc and formats disc data under control of the Disc Sequencer. In addition to these functions, this card has a data buffer which has sufficient capacity to store one complete disc track of data. This is used to give the control computer access to the data stored on the disc and also to enable the computer to write data such as directories onto the disc.

2. CIRCUIT DESCRIPTION

The disc controller system runs on a 1MHz clock. This is obtained from a divide by eight counter, GE. The 8MHz clock to this counter can come from one of three sources, selected by FE under control of the sequencer. When a disc transfer is not taking place, the clocks are switched to an on-card 8MHz source, MC. During writes to the disc, the servo clock is used as the 8MHz source and during reads from the disc, the disc read clock is used.

Serial data being read from the disc is clocked into CD and BD. The parallel output of CD shift register feeds CE which strobes the data at an appropriate time to give de-serialised data at 1M byte per second. The parallel outputs of CD and BD feed AE and AD which strobes the data at an appropriate time to give deserialised data 500k words per second. The output of CD also feeds DE and EE which act as a sync word detector. When data is written to the disc a sync word is written at the beginning of each track to enable the deserialiser to lock to the appropriate "frame" of 8-bits. A second sync word is written at the end of a track in order to check for framing errors. The sync word detector is armed by the sequencer by sending a clear pulse to KA13 which enables EE. When a sync word appears across the parallel output of CD, EE9 goes low which in turn sends KA5 low on the next 8MHz clock cycle. At this time, the sync word has been shifted down so EE9 will return to its high state. At the next clock cycle KA5 goes high again, disabling the sync detector by clocking KA8 low. Meanwhile, GE has been preset with the load pulse from KA5, which has now phased up the byte clock with the serial data stream.

LE, KE and ME count the 1MHz byte per second clocks and only allow clocks to be output which correspond to valid picture points, totalling 768 per line.

HD is used to serialise data when writing to the disc. LD is used to generate a load pulse after a positive transition of the byte clock. The 8-bits of data are then shifted out with the 8MHz bit clock. Data can be supplied from several sources (under control of the sequencer) detailed below.

(a) GD provides a source of all zeros which is used to write gaps preceeding the sync word and between the sync word and data on the disc.

(b) FD provides the sync word pattern.

(c) CC and DC enable the 16-bits of decoded video data from the control bus.

(d) ED enables data in the RAM buffer store to be output to the disc.

AA, BB and BA buffer the control bus. DB decodes CSR codes 0, 1 and 7, LA9 holds the tape mode bit of the computer status word. It is used to route data from the disc onto the control bus, via DD in tape mode. With CSR code 1 selected (disc command word) BC is enabled, which then decodes the top 4-bits of the control word. If this has a value of two a disc transfer command has been issued and the R/W bit is stored at LA5. In read mode this is low which puts a permanent clear on output shift register HD which reduces the noise pick up on the disc radial cable. LA6 is used to gate the enable of DD so that it is only enabled during disc reads when in tape mode. If the top 4-bits of the control word have a value of 1, "preset RAM address" command has been issued. This causes KD6 to go low which feeds the load inputs of the RAM address counters JA, IA, FA and EA. It also triggers MD1 which provides a clock for the counters while their load input is low. The address to which the counters need to be preset appears on the lower 12-bits of the control bus.

With CSR code seven selected, the control computer has the ability to read from or write to the data buffer RAM. When reading from the RAM TX/RX goes low and data out of the RAM is enabled onto the eight least significant data lines of the control bus with CA. When the control computer has read a byte it pulses DTX which clocks the RAM address counters to the next address. When writing to the RAM an NDR is generated at LC8. This clocks the data on the eight least significant data lines of the control bus into DA. It also triggers monostables MD9 and NA1. MD enables data to the RAMs while NA pulses the write enable pin of the RAMs. The latter also serves to clock the RAM address counters onto the next address via JE12.

The sequencer has control of the RAM with signals READ RAM, WRITE RAM and ZERO RAM ADDRESS. When READ RAM is pulsed ED is enabled, routing the RAM output to the data serializer. This signal also feeds JE2 which clocks the RAM address counters. When WRITE RAM is pulsed DD is enabled, routing data from the disc to the RAM. This signal also pulses the write enable line on the RAM and clocks the RAM address counters via JE10. ZERO RAM ADDRESS simply clears the RAM address counters.

GA goes high when an address count of 19200 is reached. Links have been provided for possible future extension. This signal is fed back to the sequencer, flagging that a complete track of data has been transferred from or to the RAM. This number is made identical to the number of picture points stored on a track in video mode. This allows all tracks to be written or read as data or video which gives the control computer the ability to add title information onto the end of a video track.

CAPACITORS

REF.	DESCRIPTION	STOCK CODE
C1-C2	47pF, 100V, 10%	03/06/0047
C3-C4	100pF, 100V, 10%	03/06/0306
C5	47pF, 100V, 10%	03/06/0047
C6	33pF, 100V, 10%	03/06/0489
C7-C8	47pF, 100V, 10%	03/06/0047
C9	22µF, 16V, 20%	03/03/0253
C10-C77	100000pF, 50V, +80 -20%	03/06/0233
C78	220pF, 100V, 10%	03/06/0055

RESISTORS

REF.	DESCRIPTION	STOCK CODE
R1	220Ω x 7, 125mW, 5%, 300ppm	01/08/1705
R2	4.7kΩ, 25mW, 1%, 50ppm	01/01/2177
R3	18kΩ, 25mW, 1%, 50ppm	01/01/0999
R4	10kΩ, 25mW, 1% 50ppm	01/01/2207
R5-R7	4.7kΩ, 25mW, 1%, 50ppm	01/01/2177
R8	100Ω, 25mW, 1% 50ppm	01/01/0328
R9	220Ω, 25mW, 1%, 50ppm	01/01/0441

INTERGRATED CIRCUITS

REF.	DESCRIPTION	STOCK CODE
AA	74LS244	04/01/2828
AB,AC	74LS240	04/01/2879
AD,AE	74LS374	04/01/3328
BA,BB	74LS244	04/01/2828
BC	74LS138	04/01/109Y
BD	74LS164	04/01/3719
BE	74LS244	04/01/2828
CA,CC	74LS244	04/01/2828
CD	74LS164	04/01/3719
CE	74LS374	04/01/3328
DA	74LS374	04/01/3328
DB	74LS138	04/01/109Y
DC,DD	74LS244	04/01/2828
DE	74LS240	04/01/2879
EA	74LS161	04/01/1287
EB,EC	MOS6116-3	04/01/345Y

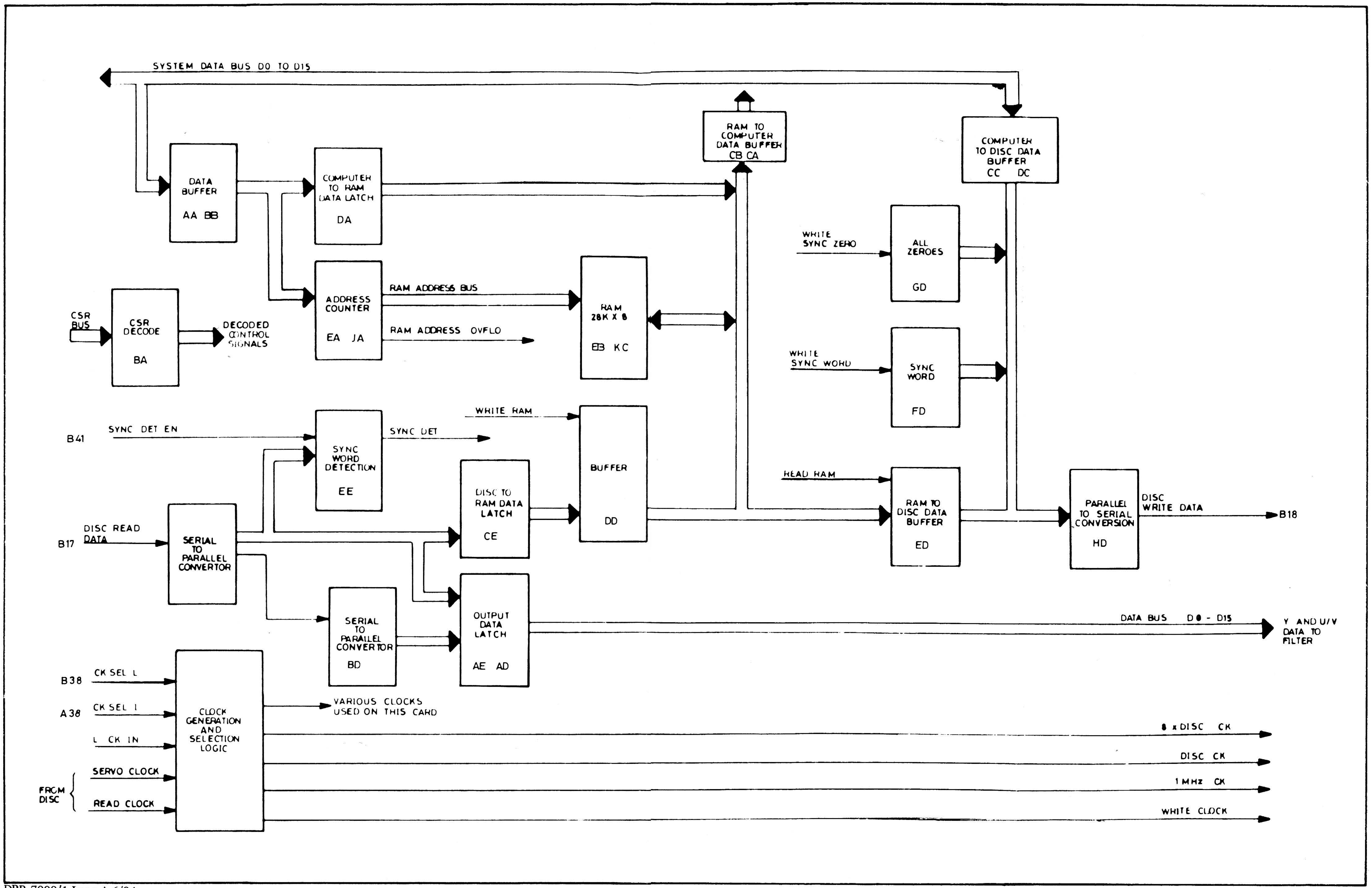
INTEGRATED CIRCUITS (Cont.)

REF.	DESCRIPTION	STOCK CODE
ED	74LS244	04/01/2828
EE	74S133	04/01/3638
FA	74LS161	04/01/1287
FB,FC	MOS6116P-3	04/01/345Y
FD	74LS244	04/01/2828
FE	74S153	04/01/3638
GA	74LS21	04/01/345X
GB-GC	MOS6116P-3	04/03/345Y
GD	74LS244	04/01/2828
GE	74LS161	04/01/1287
HA	74154N	04/01/1198
HB,HC	MOS 6116P-3	04/03/345Y
HD	74LS166	04/01/319Y
HE	74S74N	04/01/0698
HF	74LS08N	04/01/417Y
IA	74LS161A	04/01/1287
IB,IC	MOS 6116P-3	04/03/345Y
ID	74LS20PN	04/01/3093
IE	74S32N	04/01/0485
JA	74LS161A	04/01/1287
JB,JC	MOD 6116P-3	04/01/345Y
JD	74LS04N	04/01/0191
JE	74LS221N	04/01/1589
KA	74LS74N	04/01/0728
KB,KC	MOS 6116P-3	04/01/345Y
KD	74LS00N	04/01/006X
KE	74LS161A	04/01/1287
LA	74LS74N	04/01/0728
LB	74LS32N	04/01/3506
LC	74LS08N	04/01/417Y
LE	74LS161A	04/01/1287
MA	74LS10N	04/01/3123
MB	74LS08N	04/01/417Y
MC	74S124N	04/01/1031
MD	74LS221N	04/01/1589
ME	74LS161A	04/01/1287
NA	74LS221N	04/01/1589
NE	74LS74N	04/01/0728

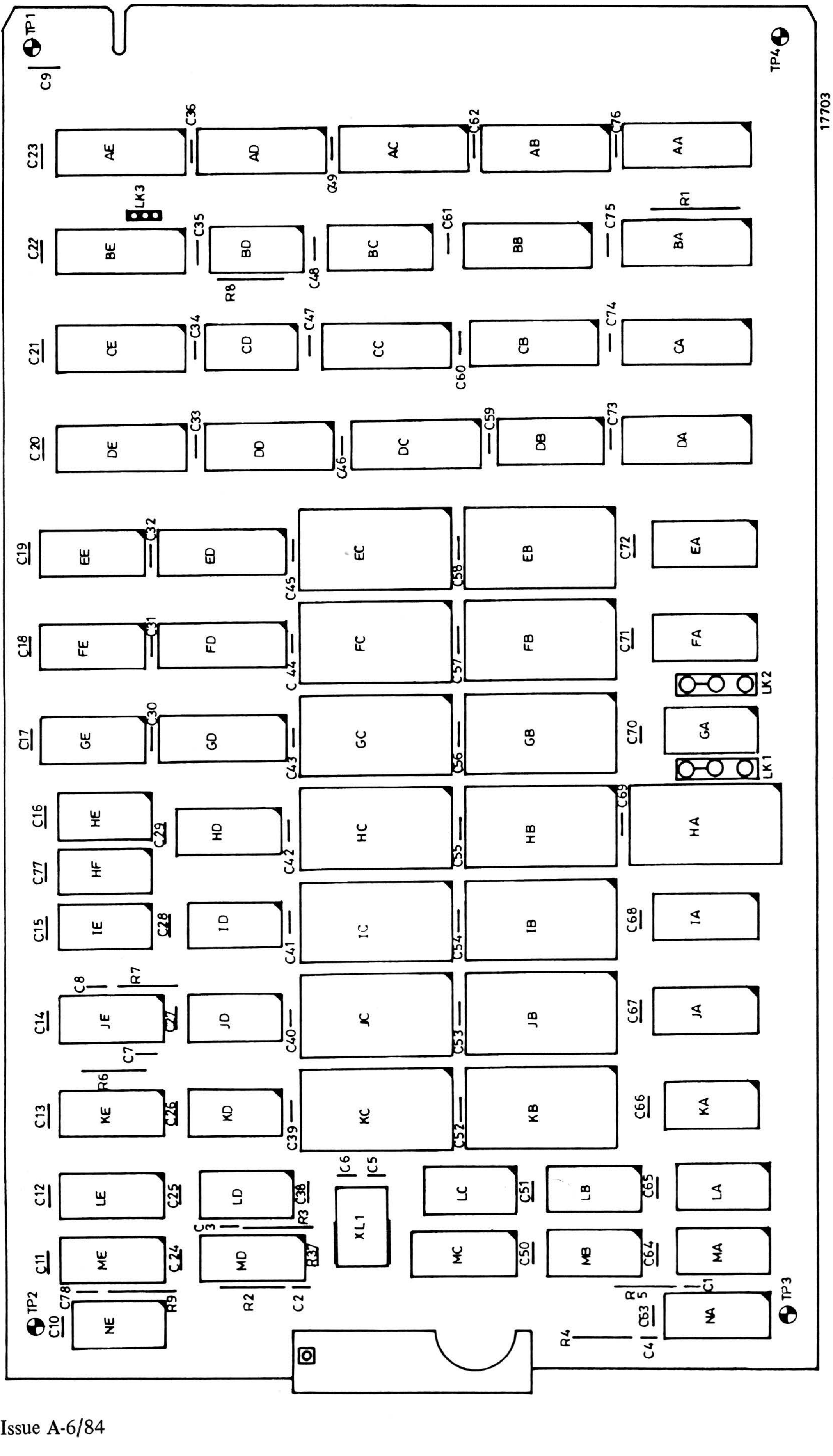
MISCELLANEOUS

REF.	DESCRIPTION	STOCK CODE
LK1,LK2	Link, Blue	18/02/013Y
XL1	Crystal Oscillator	28/01/0508

17703 Component List



17703 Figure 1 Disc Data Buffer Card Block Diagram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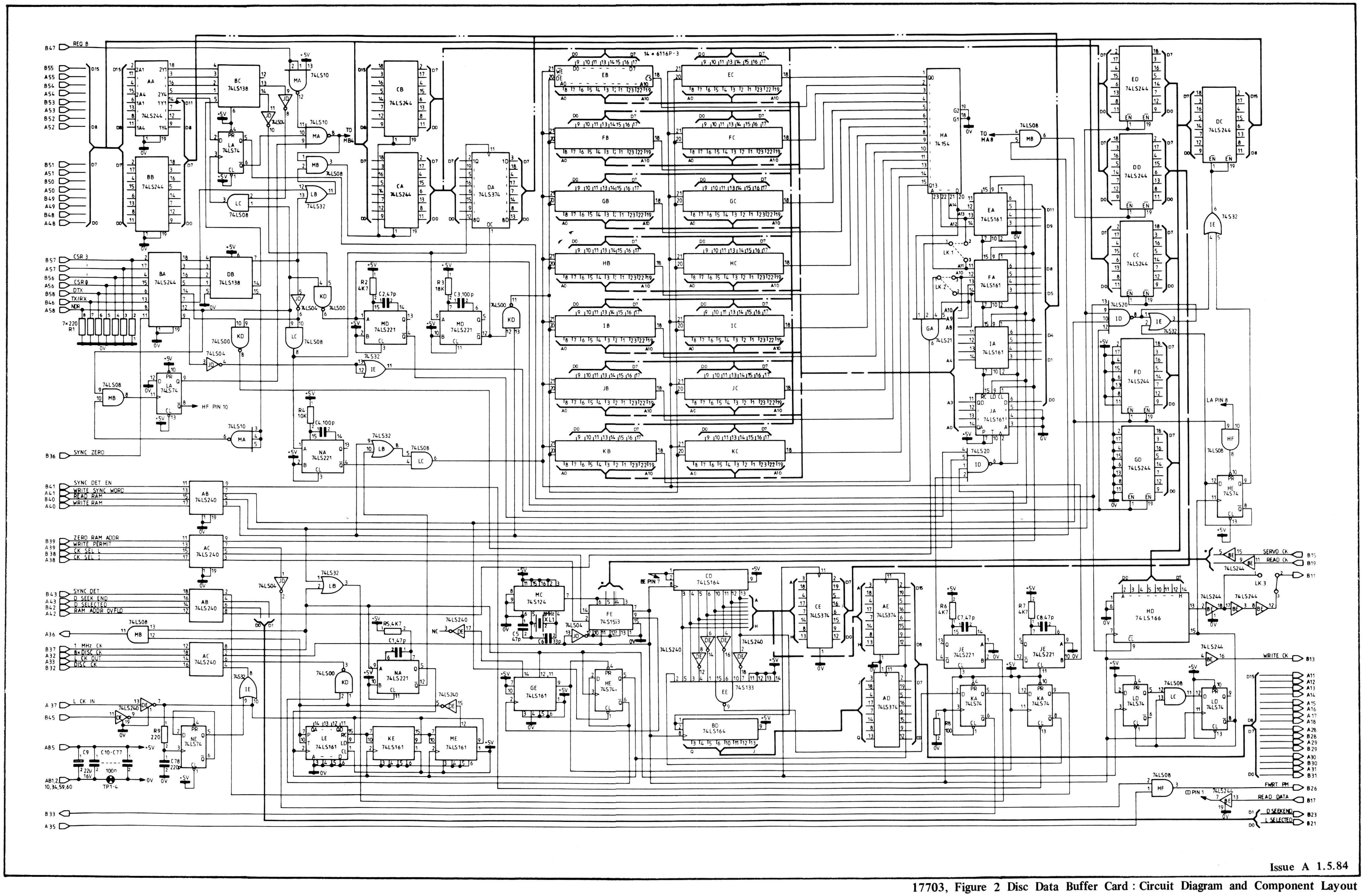
TP2
TP3
TP4
17703
C9
C23
AE
C36
AD
C49
AC
C62
AB
C76
AA
LK3
C22
BE
C35
BD
R8
C48
BC
C61
BB
C75
BA
R1
C21
CE
C34
CD
C47
CC
C60
CB
C74
CA
C20
DE
C33
DD
C46
DC
C59
DB
C73
DA
C19
EE
C32
ED
C45
EC
C58
EB
C72
EA
C18
FE
C31
FD
C44
FC
C57
FB
C71
FA
LK2
C17
GE
C30
GD
C43
GC
C56
GB
C70
GA
LK1
C16
HE
C29
HD
C42
HC
C55
HB
C69
HA
C77
HF
C15
IE
C28
ID
C41
IC
C54
IB
C68
IA
C8
R7
C14
JE
C27
JD
C40
JC
C53
JB
C67
JA
C7
R6
C13
KE
C26
KD
C39
KC
C52
KB
C66
KA
C12
LE
C25
LD
C38
C6
C5
XL1
LC
C51
LB
C65
LA
C3
R3
C11
ME
C24
MD
R37
MC
C50
MB
C64
MA
C78
R9
R2
C2
R5
C1
C10
NE
R4
C63
C4
NA



Issue A 1.5.84

17703, Figure 2 Disc Data Buffer Card : Circuit Diagram and Component Layout

S.M.D. INTERFACE : CONTROL CARD 17304
AND EXTENSION CARD 17305

1. INTRODUCTION

These cards provide a driving interface between the disc sequencer and up to four disc drives. The SMD Interface, 17304 provides the daisy chain control signals and a single data transfer radial connection. The Extension card, 17305 provides another three data transfer radial connections.

2. CIRCUIT DESCRIPTION

These are the rear facing cards carrying the disc sockets. There are four possible configurations:–

For one disc, use 1 x 17304

For two, three or four discs, use 1 x 17304 and 1 x 17305

For five discs, use 2 x 17304 and 1 x 17305

For six, seven or eight discs, use 2 x 17304 and 2 x 17305

Each disc is connected to the S.M.D. Interface by two cables, a 60-way BUS cable (which joins up to four discs in a daisy chain fashion), and a 26-way RADIAL cable (unique to individual discs). All signals on these cables use complementary current drive. The function of the S.M.D. Interface cards is:–

(a) To provide the necessary interface between this standard and T.T.L. as used within the machine, and

(b) to distribute the signals amongst discs as appropriate.

3. BUS SIGNALS (17304)

A 2-bit select code (which is used to select one out of four discs) and a 10-bit code with three tags (which select the cylinder, head and command required) are transmitted down both BUS cables to all discs connected. Some types of disc can accept 3-bit select code, but others can only accept a 2-bit code. So as to suit either type, the third select bit (on B31) operates internally, whilst the output bit is tied high (BG pins 1, 2: all disc signals use inverted logic). To make this selection, B37 is left open circuit on one Control card (disc 1-4), whilst it is wired (in the rack) to 0V on the other (discs 5-8). Thus the signal at BF pin 3 goes high on whichever Control card carries the appropriate BUS connector, which:–

(a) enables the appropriate set of eight disc status signals through to the Disc Sequencer card via AG on the selected Control card;

(b) enables the select code tag and WRITE PROTECT signal onto the appropriate BUS cable; and

(c) is the signal F SEL 2 +/– on A36 for use in enabling some RADIAL signals as described below.

4. RADIAL SIGNALS (17304 AND 17305)

The SERVO CLOCK, READ DATA, READ CLOCK, WRITE SELECTED and SEEK END signals from the appropriate disc are enabled through to the Disc Data Buffer card, via AH on the selected Control card in the case of discs 1, 8, 5 or via AE, AC or AA on the selected Extension card in the case of disc 2, 3, 4 or 6, 7, 8 respectively by the eight signals DISC SELECT 1 to DISC SELECT 8 from the Disc Sequencer card. The WRITE DATA and WRITE CLOCK signals are enabled onto the four RADIAL cables associated with the selected BUS cable by the signal F SEL 2 +/– derived as described above. It is unnecessary to be any more selective than this as the unit select code will ensure that only one disc responds to these signals.

REF.	DESCRIPTION	STOCK CODE
CAPACITORS		
C1, C2	47μF, 16V, 20%	03/03/027X
C3-C33	100000pF, 50V, +80%-20%	03/06/0233
C34	1000pF, 100V, 10%	03/06/0314
C35-C46	100000pF, 50V, +80%-20%	03/06/0233
C47, C48	1000pF, 100V, 10%	03/06/0314
C49-C53	2200pF, 100V, 20%	03/06/0152
RESISTORS		
R1, R2	1kΩ, 250mW, 2%, 100ppm	01/01/0646
R3	10kΩ, 250mW, 2%, 100ppm	01/01/0948
R4	1kΩ, 250mW, 2%, 100ppm	01/01/0646
R5, R6	56Ω, 250mW, 2%, 100ppm	01/01/0239
R7, R8	470Ω, 250mW, 2%, 100ppm	01/01/0557
R9-R12	56Ω, 250mW, 2%, 100ppm	01/01/0239
R13	1kΩ, 250mW, 2%, 100ppm	01/01/0646
R14	10kΩ, 250mW, 2%, 100ppm	01/01/0948
R15	1kΩ, 250mW, 2%, 100ppm	01/01/0646
INTEGRATED CIRCUITS		
AA-AD	500Ω, 5V	09/01/0211
AF	Dil Switch	09/01/0211
AG, AH	74LS244N	04/01/2828
BA-BD	75110AN	
BF	74LS86N	04/01/0833
BG, BH	75110AN	
CC, CD	470Ω x 8, 250mW, 2%, 100ppm	01/08/1586
CE-CG	75107AN	04/01/166X
DA-DD	56Ω x 15, 125mW, 2Ω, 100ppm	01/08/1594
DE	470Ω x 8, 250mW, 2%, 100ppm	01/08/1586
DF-DH	75107AN	04/01/166X

17304 Component List

REF.	DESCRIPTION	STOCK CODE
CAPACITORS		
C1, C2	47µF, 16V, 20%	03/03/027X
C3-C29	100000pF, 50V, +80%-20%	03/06/0233
RESISTORS		
R1	1kΩ, 250mW, 2%, 100ppm	01/01/0646
R2, R3	470Ω, 250mW, 2%, 100ppm	01/01/0557
R4	1kΩ, 250mW, 2%, 100ppm	01/01/0646
R5, R6	470Ω, 250mW, 2%, 100ppm	01/01/0557
R7	1kΩ, 250mW, 2%, 100ppm	01/01/0646
R8, R9	470Ω, 250mW, 2%, 100ppm	01/01/0557
INTEGRATED CIRCUITS		
AA	74LS244N	04/01/2828
AB	75110AN	04/01/1686
AC	74LS244N	04/01/2828
AD	75110AN	04/01/1686
AE	74LS244N	04/01/2828
AF	75110AN	04/01/1686
BA-CE	75107AN	04/01/166X

17305 Component List

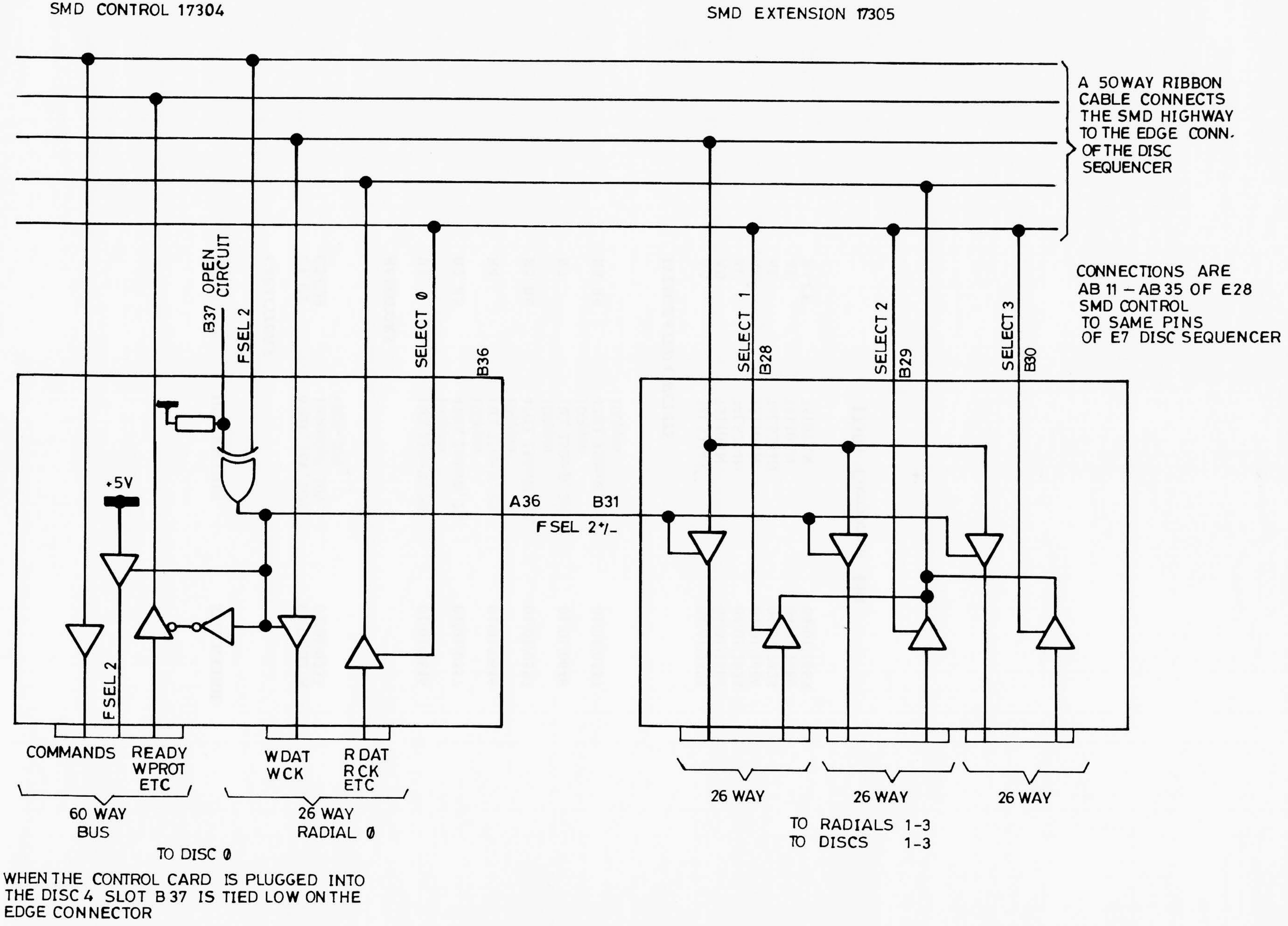

SMD CONTROL 17304
SMD EXTENSION 17305
A 50WAY RIBBON CABLE CONNECTS THE SMD HIGHWAY TO THE EDGE CONN. OF THE DISC SEQUENCER
CONNECTIONS ARE AB 11 – AB 35 OF E28 SMD CONTROL TO SAME PINS OF E7 DISC SEQUENCER
B37 OPEN CIRCUIT
FSEL 2
SELECT 0
B36
+5V
A36
B31
FSEL 2+/–
SELECT 1
B28
SELECT 2
B29
SELECT 3
B30
FSEL 2
COMMANDS
READY
WPROT
ETC
WDAT
WCK
RDAT
RCK
ETC
60 WAY
BUS
26 WAY
RADIAL 0
TO DISC 0
WHEN THE CONTROL CARD IS PLUGGED INTO THE DISC 4 SLOT B 37 IS TIED LOW ON THE EDGE CONNECTOR
26 WAY
26 WAY
26 WAY
TO RADIALS 1-3
TO DISCS 1-3

Figure 1 SMD Interface Connections

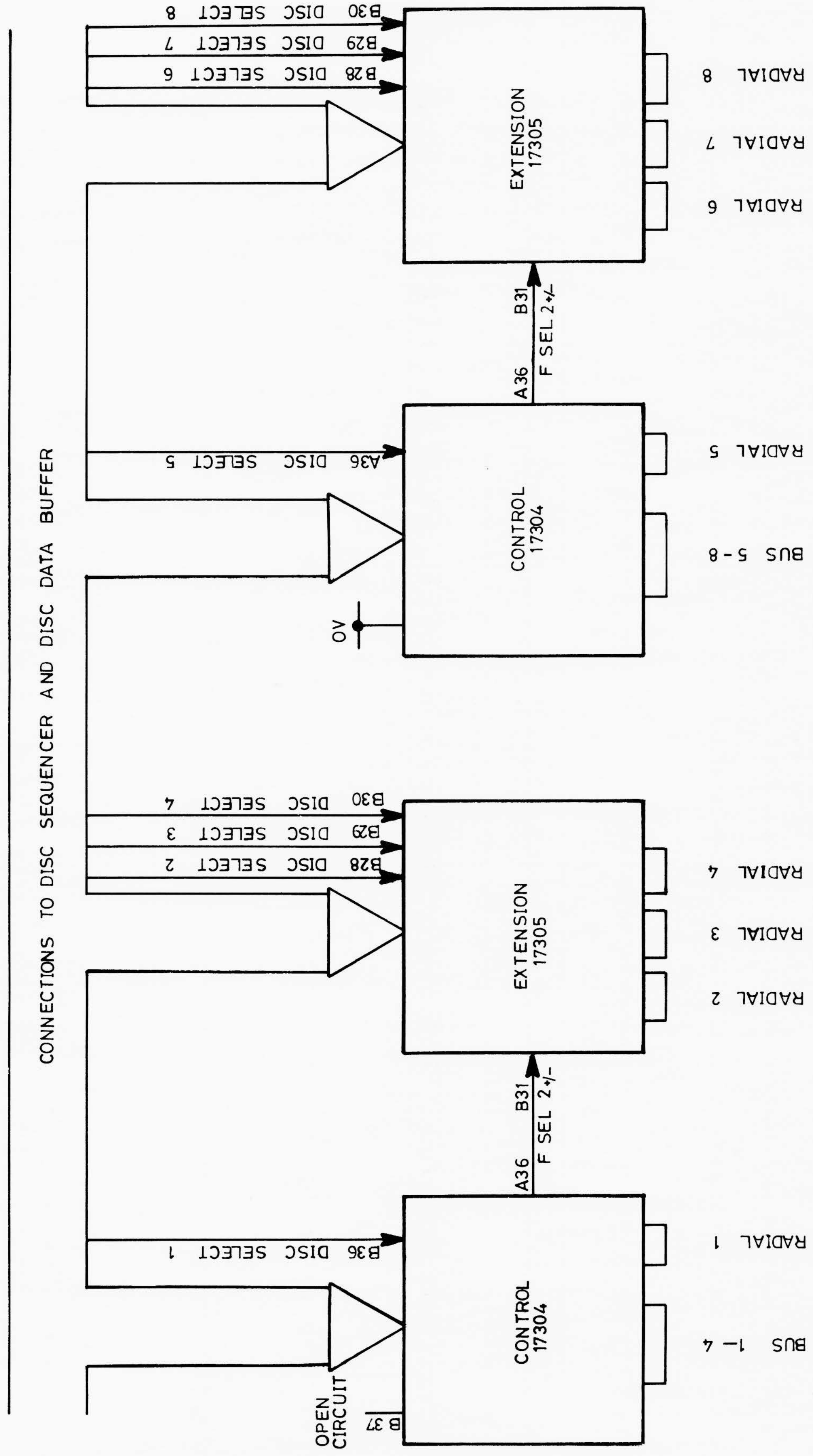
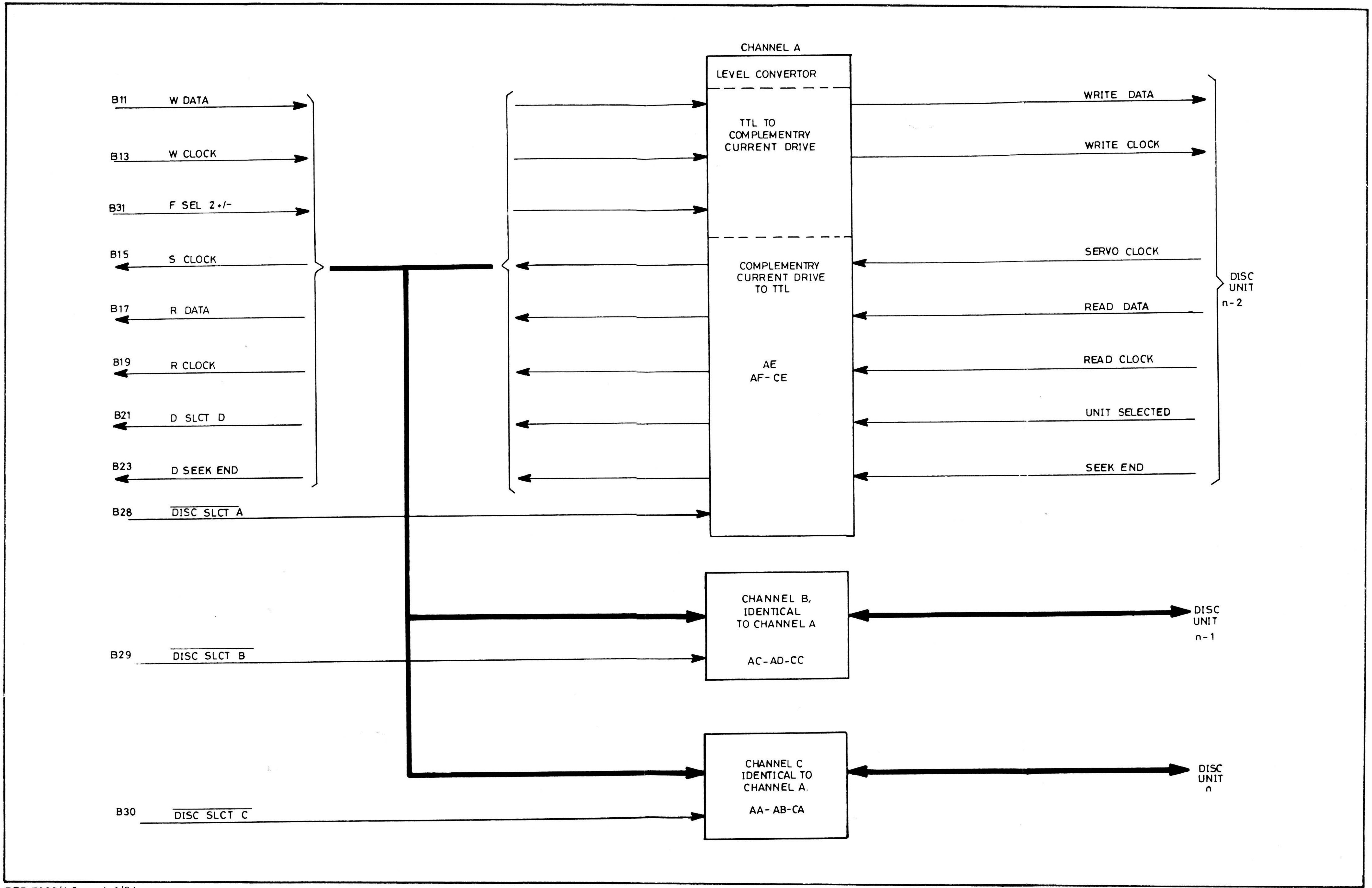
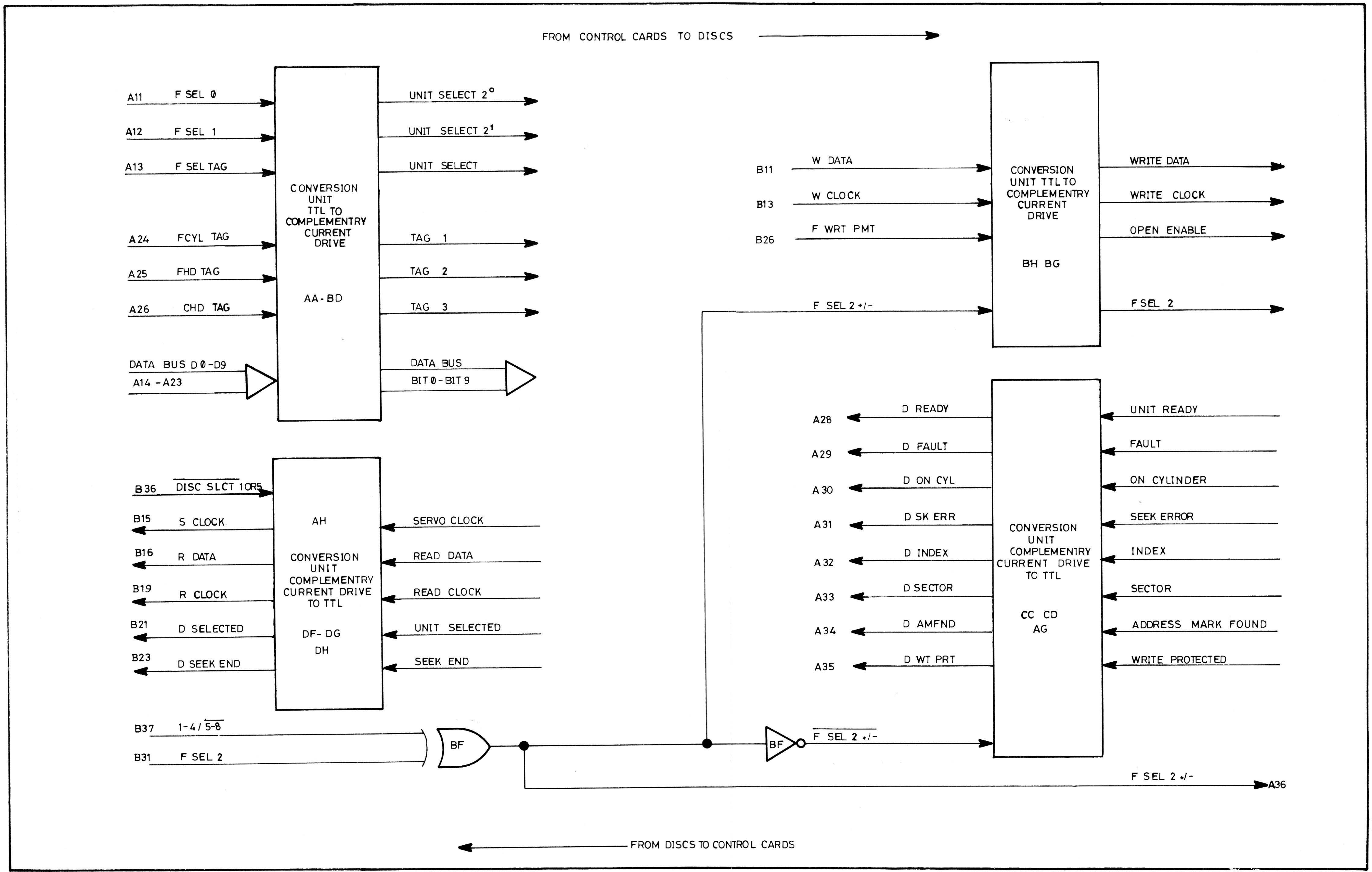


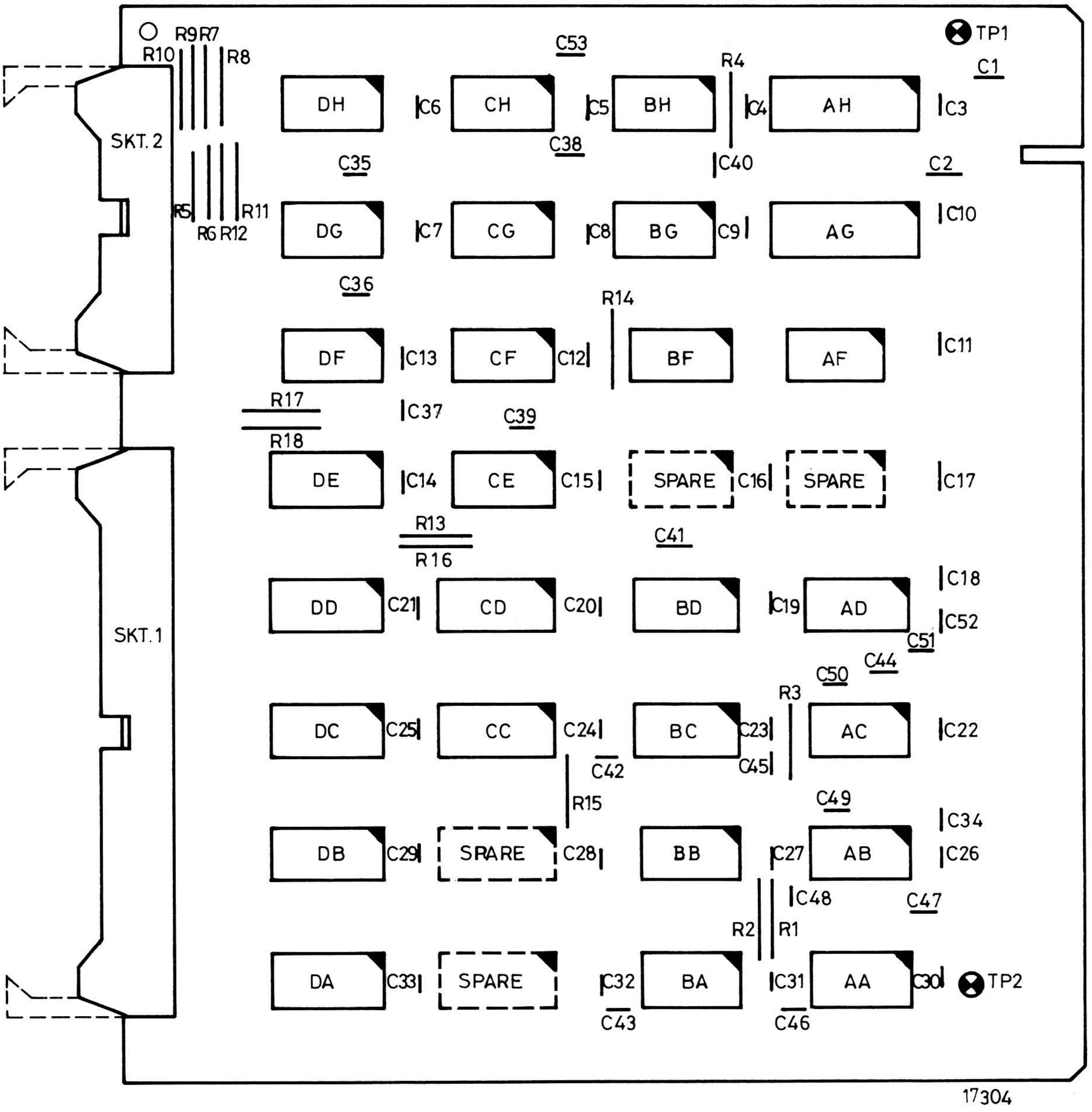
Figure 2 SMD Interface Block Diagram

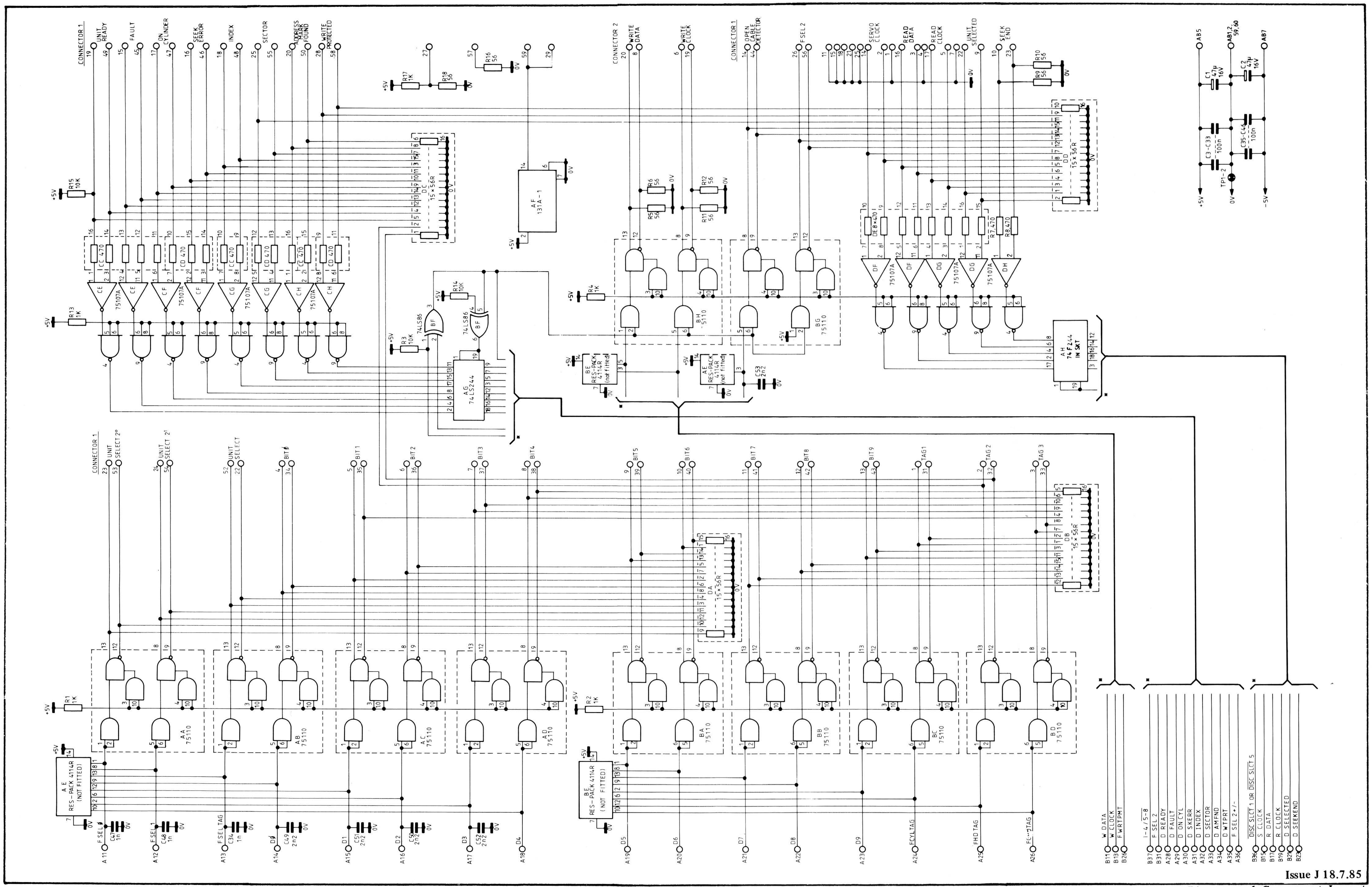


17305, Figure 3 SMD Interface Extension Card Block Diagram



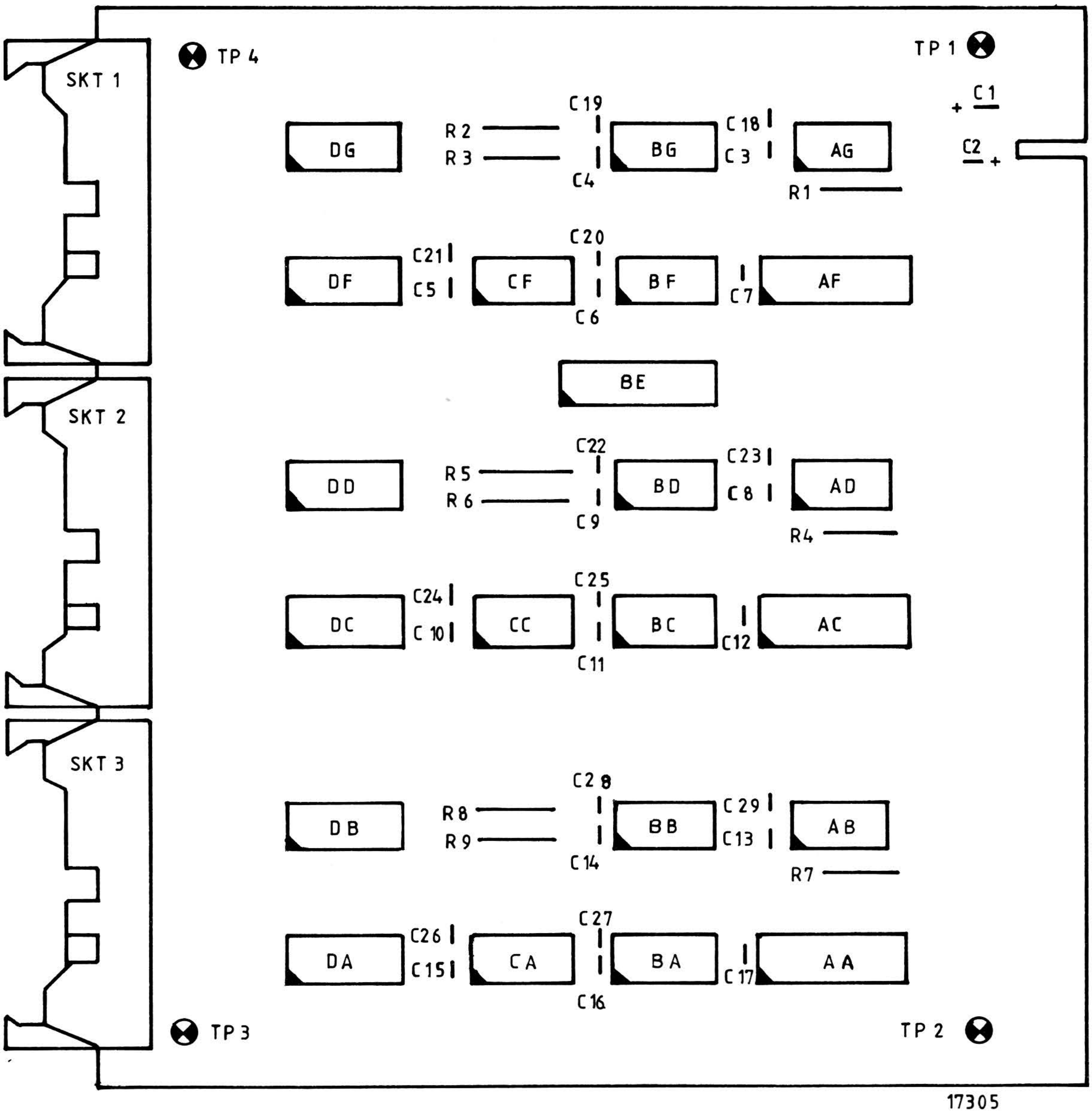
17304, Figure 4 SMD Interface Control Card Block Diagram

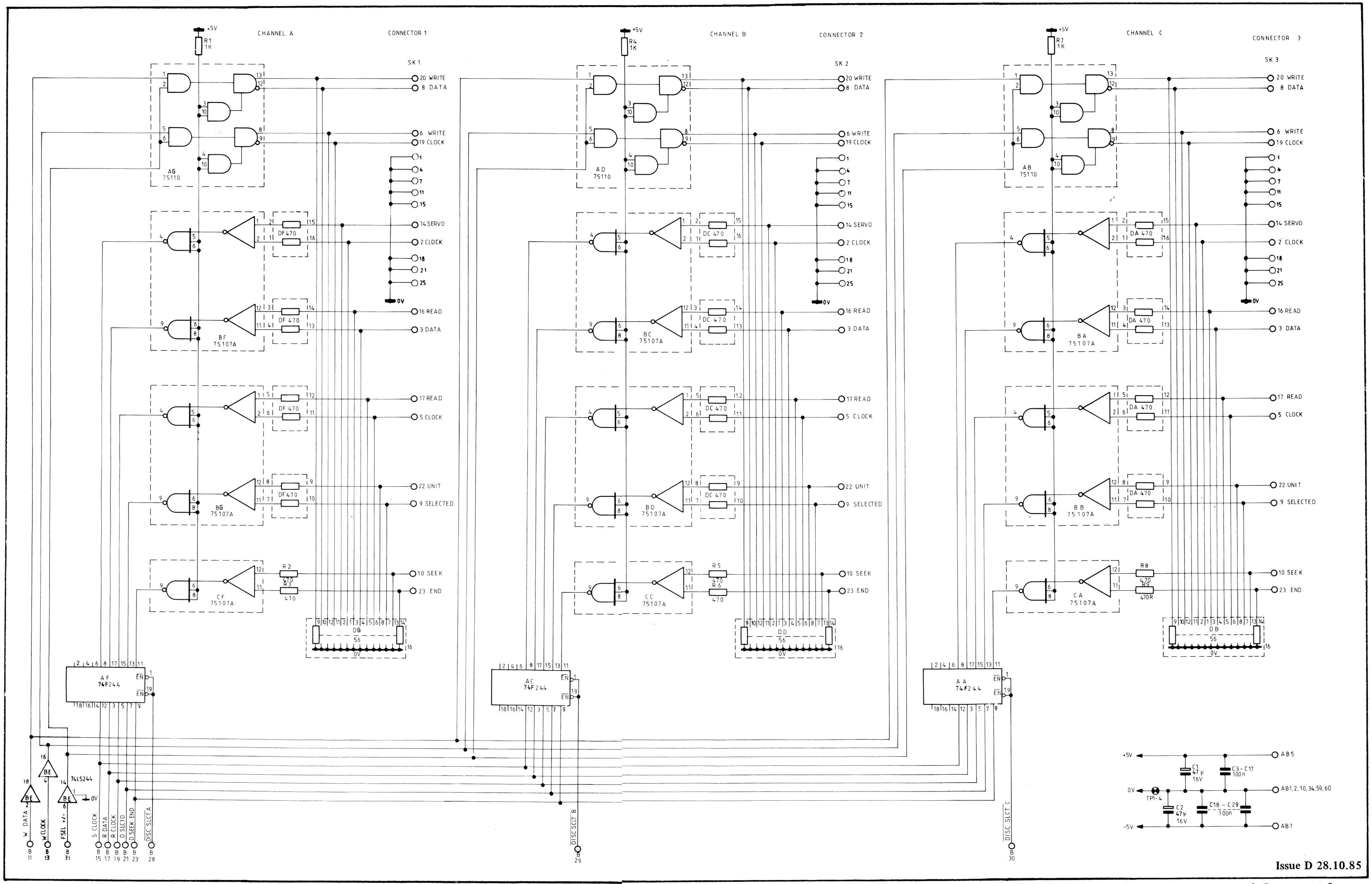

TP1
R9 R7
R10
R8
C53
R4
C1
SKT. 2
DH
C6
CH
C5
BH
C4
AH
C3
C38
C35
C40
C2
R5
R6 R12
R11
DG
C7
CG
C8
BG
C9
AG
C10
C36
R14
DF
C13
CF
C12
BF
AF
C11
R17
R18
C37
C39
DE
C14
CE
C15
SPARE
C16
SPARE
C17
R13
R16
C41
C18
SKT. 1
DD
C21
CD
C20
BD
C19
AD
C52
C51
C44
C50
R3
DC
C25
CC
C24
BC
C23
AC
C22
C42
C45
R15
C49
C34
DB
C29
SPARE
C28
BB
C27
AB
C26
C48
C47
R2
R1
DA
C33
SPARE
C32
BA
C31
AA
C30
TP2
C43
C46
17304



Issue J 18.7.85

17304 Figure 5 SMD Interface Control Card : Circuit Diagram and Component Layout


SKT 1
SKT 2
SKT 3
TP 1
TP 2
TP 3
TP 4
C1
C2
DG
R2
R3
C19
C4
BG
C18
C3
AG
R1
DF
C21
C5
CF
C20
C6
BF
C7
AF
BE
DD
R5
R6
C22
C9
BD
C23
C8
AD
R4
DC
C24
C10
CC
C25
C11
BC
C12
AC
DB
R8
R9
C28
C14
BB
C29
C13
AB
R7
DA
C26
C15
CA
C27
C16
BA
C17
AA
17305



Issue D 28.10.85

17305, Figure 6 SMD Interface Extension Card : Circuit Diagram and Component Layout

FILTER CARD

17427

1. INTRODUCTION

This card is situated in the data path between the disc and the painting stores. The card performs the horizontal, vertical and rotation filtering to correct the effects of size and axis changes on a picture.

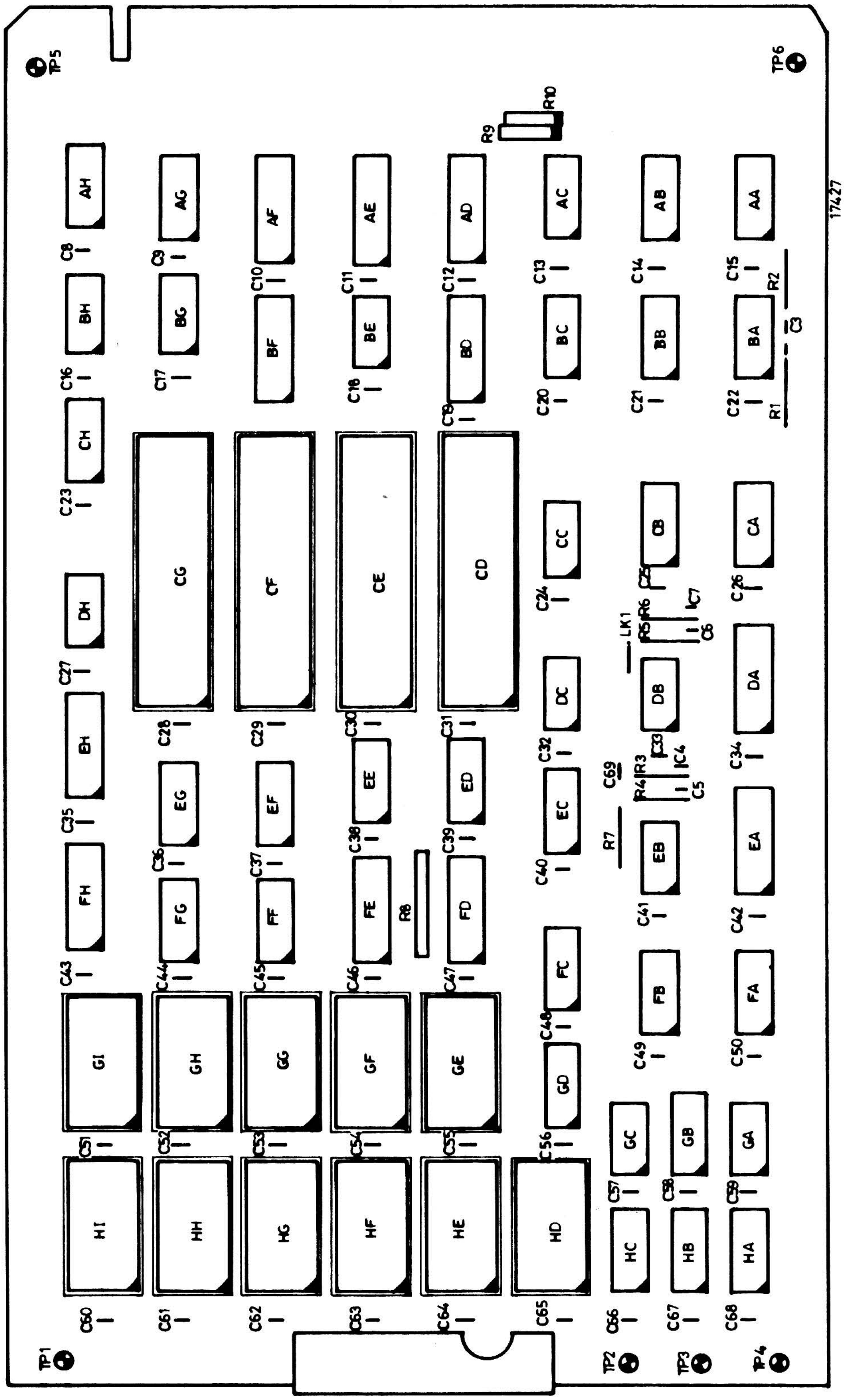
2. CIRCUIT DESCRIPTION

Should this card be faulty please return it to Quantel for repair.

REF.	DESCRIPTION	STOCK CODE
CAPACITORS		
C1	22μF, 16V, 20%	03/03/0253
C2,C3	68μF, 100V, 10%	03/06/0497
C4	47pF, 100V, 10%	03/06/0047
C5	180pF, 100V, 5%	03/06/042X
C6	47pF, 100V, 10%	03/06/0047
C7	180pF, 100V, 5%	03/06/042X
C8-C68	100000pF, 50V, +80% −20%	03/06/0233
C69	220pF, 100V, 10%	03/06/0055
RESISTORS		
R1,R2	3.9kΩ, 250mW, 2%, 100ppm	01/01/0808
R3	150Ω, 250mW, 2%, 100ppm	01/01/0387
R4	220Ω, 250mW, 2%, 100ppm	01/01/0441
R5	150Ω, 250mW, 2%, 100ppm	01/01/0387
R6,R7	220Ω, 250mW, 2%, 100ppm	01/01/0441
R8	1kΩ x 8, 125mW, 5%, 300ppm	01/08/0539
R9,R10	1kΩ x 4, 125mW, 5%, 300ppm	01/08/083Y
INTEGRATED CIRCUITS		
AA	74LS138N	04/01/109Y
AB,AC	27S07PC	04/01/6319
AD	74LS373N	04/01/3821
AE	74LS240N	04/01/2879
AF	Programmed Set Make From F0'ING Ref Only 2 x 04/01/5258 7694A-5	

REF.	DESCRIPTION	STOCK CODE
INTEGRATED CIRCUITS (Cont)		
AG,AH	27S07PC	04/01/6319
BA	74LS221N	04/01/1589
BB,BC	27S07PC	04/01/6319
BD	74LS373N	04/01/3921
BE	74LS00N	04/01/006X
BF	Programmed Set Make From FO'ING Ref Only 2 x 04/01/5258 7694A-5	
BG,BH	27S07PC	04/01/6319
CA	74LS157N	04/01/1236
CB	74LS163N	04/01/1317
CC	74LS164N	04/01/3719
CD-CG	1008J	04/01/5274
CH	74LS163N	04/01/1317
DA	Programmed Set Make From FO'ING Ref Only 2 x 04/01/5258 7694A-5	
DB	74LS04N	04/01/0191
DC	74LS32N	04/01/3506
EA	74S374N	04/01/4294
EB	74LS00N	04/01/006X
EC-EE	74LS157N	04/01/1236
EF,EG	27S07PC	04/01/6319
EH	74LS374N	04/01/3328
FA	74LS163N	04/01/1317
FB	74LS174N	04/01/1422
FC	74LS157N	04/01/1236
FD-FH	74LS374N	04/01/3328
GA	74LS20PN	04/01/3093
GB	74S138N	04/01/1082
GC	74LS08N	04/01/417Y
GD	74S153N	04/01/1171
GE-GI	4801AJ-3	04/03/1334
HA-HC	93S16DC	04/01/272Y
HD-HI	4801AJ-3	04/03/1334

17427 Component List


TP1
TP2
TP3
TP4
TP5
TP6
17427
R1
R2
R3
R4
R5
R6
R7
R8
R9
R10
LK1
AA
AB
AC
AD
AE
AF
AG
AH
BA
BB
BC
BD
BE
BF
BG
BH
CA
CB
CC
CD
CE
CF
CG
CH
DA
DB
DC
DH
EA
EB
EC
ED
EE
EF
EG
EH
FA
FB
FC
FD
FE
FF
FG
FH
GA
GB
GC
GD
GE
GF
GG
GH
GI
HA
HB
HC
HD
HE
HF
HG
HH
HI
C3
C4
C5
C6
C7
C8
C9
C10
C11
C12
C13
C14
C15
C16
C17
C18
C19
C20
C21
C22
C23
C24
C25
C26
C27
C28
C29
C30
C31
C32
C33
C34
C35
C36
C37
C38
C39
C40
C41
C42
C43
C44
C45
C46
C47
C48
C49
C50
C51
C52
C53
C54
C55
C56
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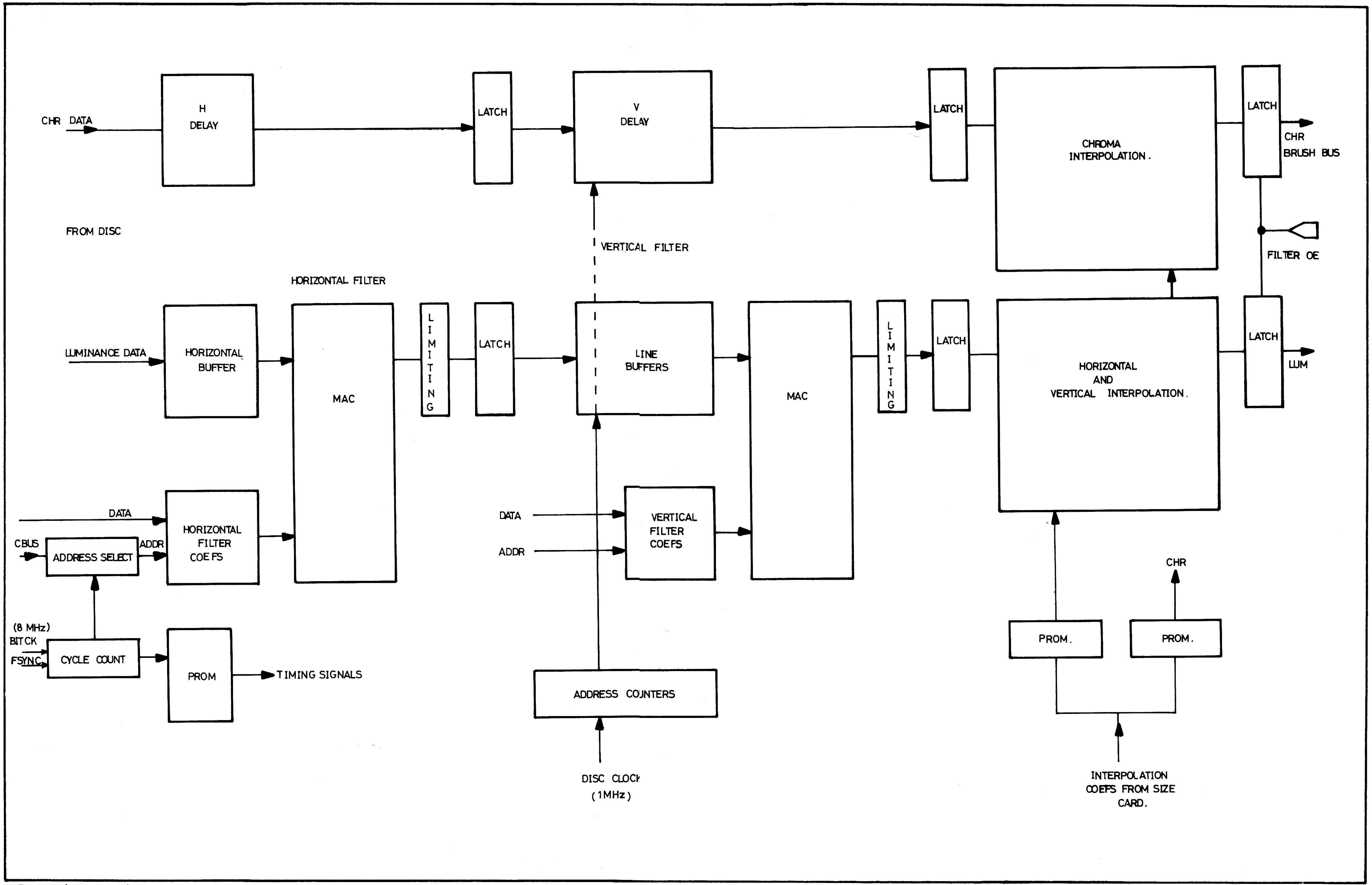
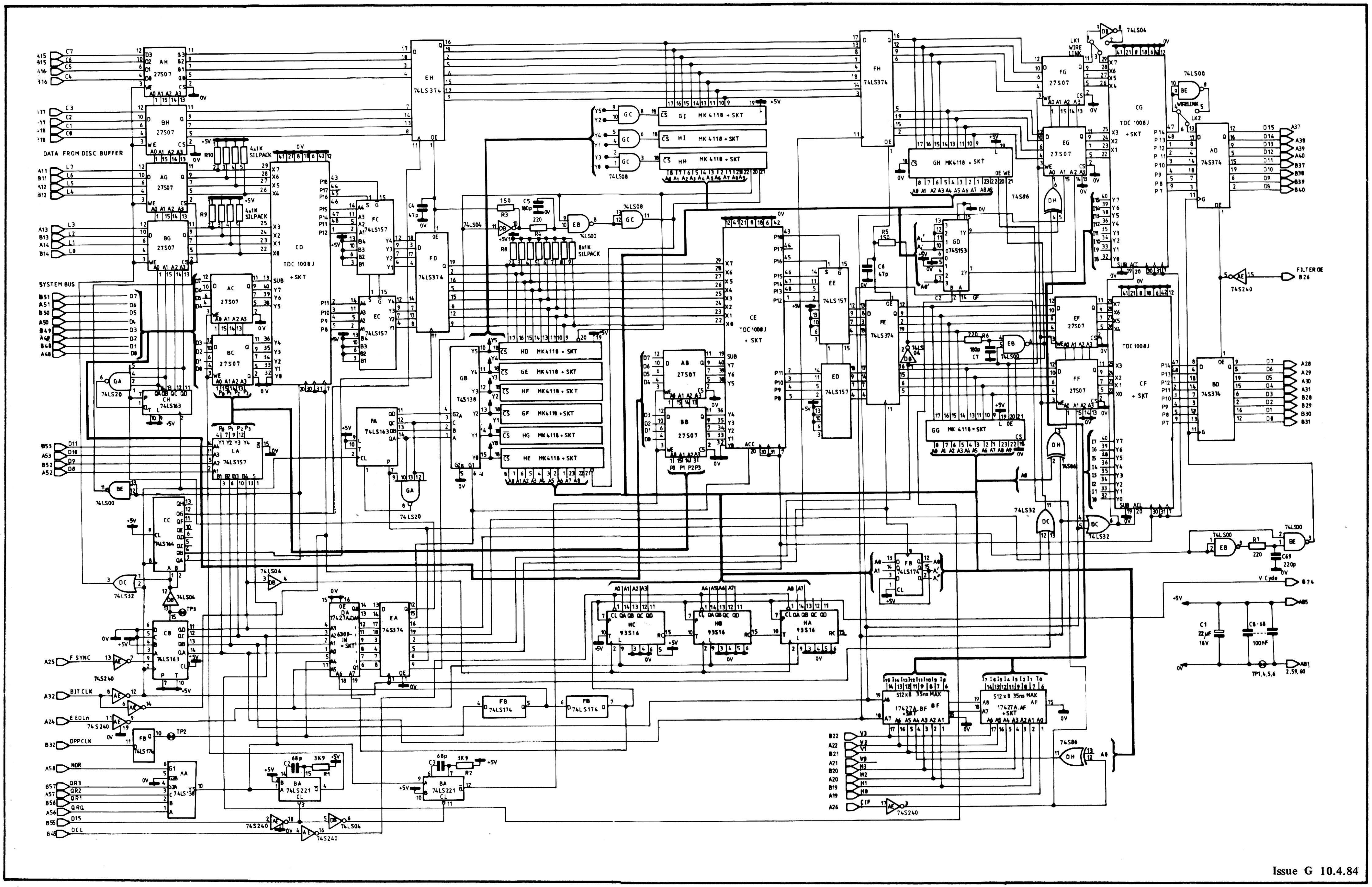
C58
C59
C60
C61
C62
C63
C64
C65
C66
C67
C68
C69



17427, Figure 1 Filter Card Block Diagram



Issue G 10.4.84

17427, Figure 2 Filter Card : Circuit Diagram and Component Layout

SIZE CARD

17428

1. INTRODUCTION

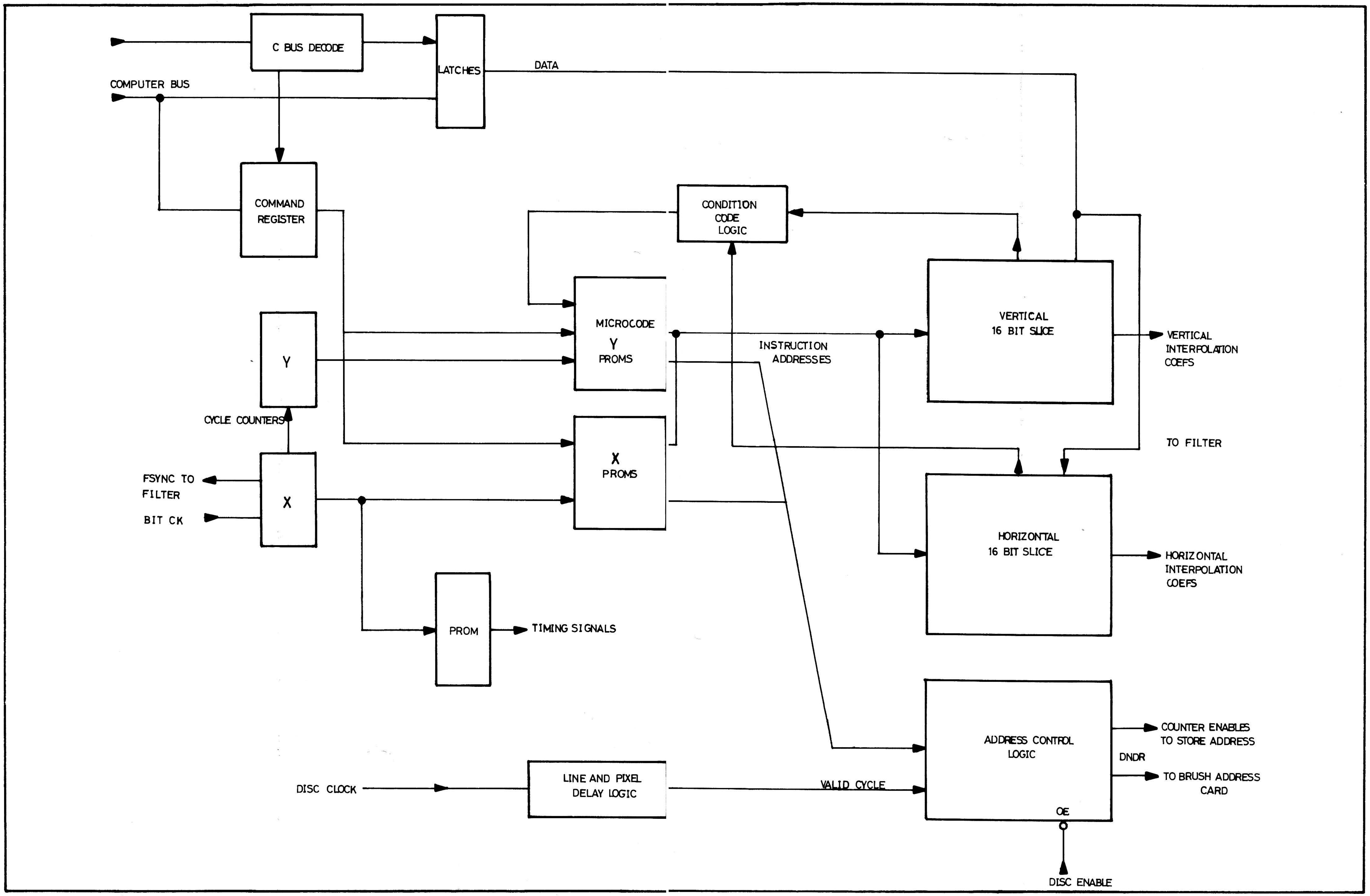
This card converts the system computer commands into store address control data and filter parameters, these provide the required size and axis referenced picture data for the painting stores.

2. CIRCUIT DESCRIPTIONS

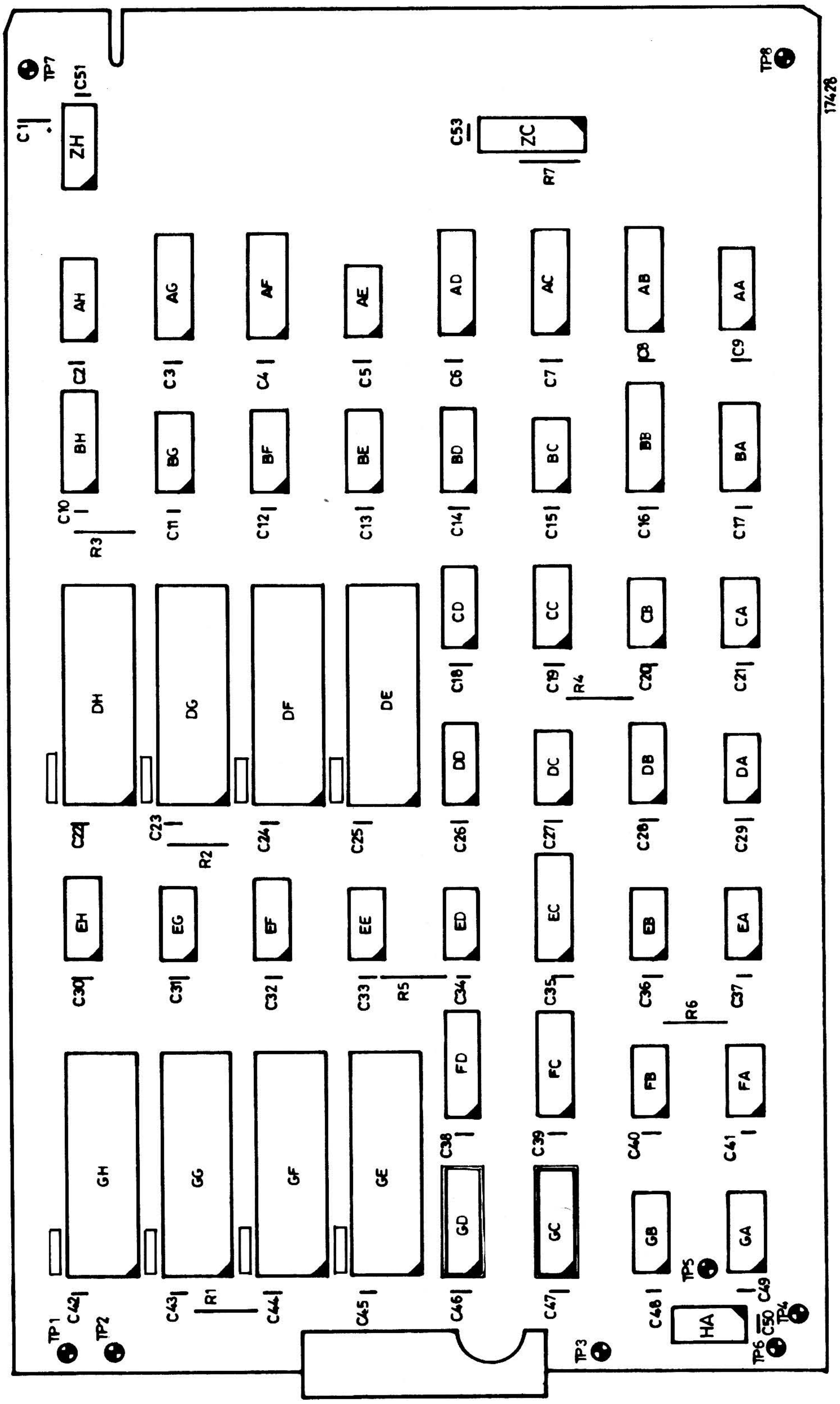
Should this card be faulty please return it to Quantel for repair.

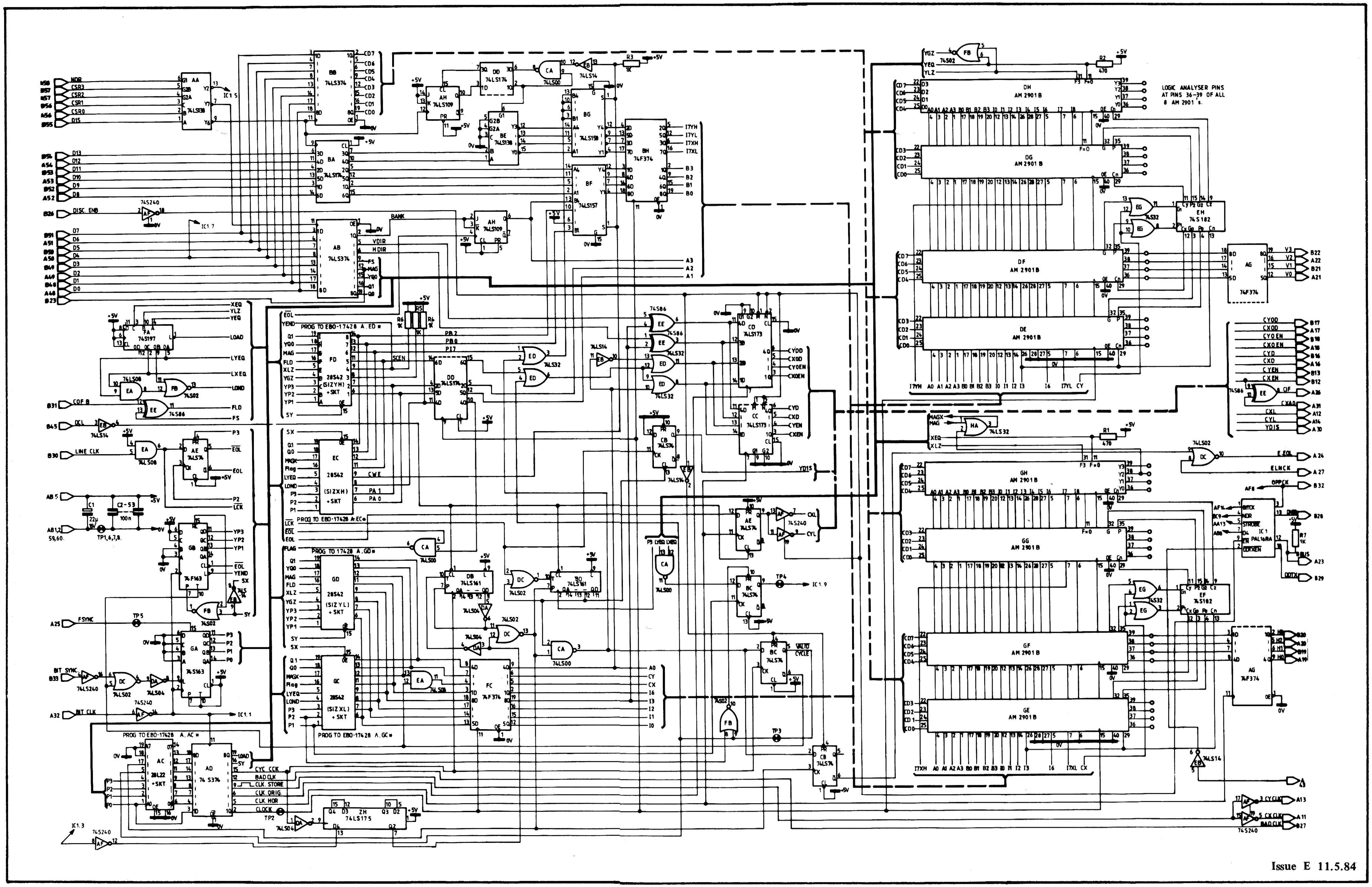
REF.	DESCRIPTION	STOCK CODE
CAPACITORS		
C1	22μF, 16V, 20%	03/03/0253
C2-C53	100000pF, 50V, +80%-20%	03/06/0233
RESISTORS		
R1, R2	470Ω, 250mW, 2%, 100ppm	01/01/0557
R3-R7	1kΩ, 250mW, 2%, 100ppm	01/01/0646
INTEGRATED CIRCUITS		
IC1	74LS240N	04/01/2879
IC2, IC3	74LS175N	04/01/1457
IC4	74LS32N	04/01/3506
AA	74LS138N	04/01/109Y
AB	74LS374N	04/01/3328
AC	Programmed set make from 1 x 4 04/04/0554 28L22 Ref. only 4 x 04/04/0953 28S42	
AD	74S374N	04/01/4294
AE	74LS74N	04/01/0728
AF	74LS240N	04/01/2879
AG	74F374PC	04/01/5592
AH	74LS109N	04/01/3166
BA	74LS174N	04/01/1422
BB	74LS374N	04/01/3328
BC	74LS74N	04/01/0728
BD	74LS161N	
INTEGRATED CIRCUITS (Cont.)		
BE	74LS138N	04/01/109Y
BF	74LS157N	04/01/1236
BG	74LS158N	04/01/3689
BH	74F374PC	04/01/5592
CA	74LS00N	04/01/006X
CB	74LS74N	04/01/0728
CC, CD	74LS173P	04/01/2836
DA	74LS04N	04/01/0191
DB	74LS161N	
DC	74LS02N	04/01/1724
DD	74LS174N	04/01/1422
DE-DH	2901BPC	04/01/3301P
EA	74LS08N	04/01/417Y
EB	74LS14N	04/01/3425
EC	Programmed set make from 1 x 4 04/04/0554 28L22 Ref. only 4 x 04/04/0953 28S42	
ED	74LS32N	04/01/3506
EE	74LS86N	04/01/0833
EF	74S182N	04/01/3735
EG	74S32N	04/01/0485
EH	74S182N	04/01/3735
FA	74S197N	04/01/5509
FB	74LS02N	
FC	74F374PC	04/01/5592
FD	Programmed set make from 1 x 4 04/04/0554 28L22 Ref. only 4 x 04/04/0953 28S42	
GA, GB	74S163N	04/01/370Y
GC, GD	Programmed set make from 1 x 4 04/04/0554 28L22 Ref. only 4 x 04/04/0953 28S42	
GE-GH	2901BPC	

17428 Component List



17428, Figure 1 Size Card Block Diagram


TP7
C51
C1
ZH
C53
ZC
R7
TP8
17428
AH
AG
AF
AE
AD
AC
AB
AA
C2
C3
C4
C5
C6
C7
C8
C9
BH
BG
BF
BE
BD
BC
BB
BA
C10
R3
C11
C12
C13
C14
C15
C16
C17
CD
CC
CB
CA
DH
DG
DF
DE
C18
C19
R4
C20
C21
DD
DC
DB
DA
C22
C23
R2
C24
C25
C26
C27
C28
C29
EH
EG
EF
EE
ED
EC
EB
EA
C30
C31
C32
C33
R5
C34
C35
C36
R6
C37
FD
FC
FB
FA
C38
C39
C40
C41
GH
GG
GF
GE
GD
GC
GB
GA
TP5
C42
C43
R1
C44
C45
C46
C47
C48
HA
C49
C50
TP4
TP6
TP1
TP2
TP3


LOGIC ANALYSER PINS AT PINS 36-39 OF ALL 8 AM 2901's.
AA 74LS138
BB 74LS374
BA 74LS374
AB 74LS374
DD 74LS174
CA 74LS00
EB 74LS14
R3 1K
AH 74LS109
BE 74LS138
BG 74LS158
BF 74LS157
BH 74F374
DH AM 2901 B
DG AM 2901 B
DF AM 2901 B
DE AM 2901 B
GH AM 2901 B
GG AM 2901 B
GF AM 2901 B
GE AM 2901 B
EH 74S182
EF 74S182
EG 74S32
AG 74F374
FB 74S02
R2 470
R1 470
HA 74LS32
IC1 PAL16R4
FA 74S197
EA 74LS08
EE 74S86
AE 74LS74
FD 28S42 (SIZYH) PROG TO EBO-17428 A.ED
EC 28S42 (SIZXH) PROG TO EBO-17428 A.EC
GD 28S42 (SIZYL) PROG TO EBO-17428 A.GD
GC 28S42 (SIZXL) PROG TO EBO-17428 A.GC
DD 74LS174
ED 74LS32
CD 74LS173
CC 74LS173
CB 74LS74
BC 74LS74
DB 74LS161
BD 74LS161
DC 74LS02
DA 74LS04
FC 74F374
GB 74F163
GA 74S163
AC 28L22 PROG TO EBO-17428 A.AC
AD 74S374
ZH 74LS175
AF 74S240
C1 22µ
C2-53 100n
TP1,6,7,8.
TP2
TP3
TP4
TP5
R4 1K
R5
R6 1K
R7 1K
B58 B57 B56 B55 B54 A54 B53 A53 B52 A52 B26 B51 A51 B50 A50 B49 A49 B48 A48 B23 B31 B45 B30 AB5 AB1,2 59,60 A25 B33 A32
MDR CSR3 CSR2 CSR1 CSR0 D15 D13 D12 D11 D10 D9 D8 DISC ENB D7 D6 D5 D4 D3 D2 D1 D0
COF B DCL LINE CLK FSYNC BIT SYNC BIT CLK
XEQ YLZ YEQ LOAD LYEQ LXEQ LOND FLD FS P3 EOL P2 LCK YP3 YP2 YP1 EOL YEND SX SY P3 P2 P1 P0
BANK VDIR HDIR FS MAG YEQ Q1 Q0 A3 A2 A1
I7YH I7YL I7XH I7XL B3 B2 B1 B0
CD7 CD6 CD5 CD4 CD3 CD2 CD1 CD0
PB2 PB0 P17 SCEN CWE PA1 PA0
CYOD CXOD CYOEN CXOEN CYD CXD CYEN CXEN YDIS
CXL CYL
MAGX MAG XEQ XLZ
A0 CY CX I6 I3 I2 I1 I0
CYC CCK BAD CLK CLK.STORE CLK.ORIG CLK.MOR CLOCK
VALID CYCLE
V3 V2 V1 V0 B22 A22 B21 A21
B17 A17 B18 A18 B16 A16 B13 B12 A26 A31 A12 A14 A30
CIF CXAD CXL CYL YDIS
E.EOL A24 ELNCK A27 OPPCK B32
B28 A23 B29 B30 A30 B19 A19
A13 A11 B27
IC1.1 IC1.3 IC1.5 IC1.7 IC1.9
+5V 0V

Issue E 11.5.84

17428, Figure 2 Size Card : Circuit Diagram and Component Layout

BRUSH ADDRESS CARD

17419

1. INTRODUCTION

The Brush Address card has the following functions:–

a) Latches a status word that determines the overall function of the machine.

b) Provides refresh, read and write access to the Brush Store

c) Provides counters that define an array size for accesses to the framestore.

d) Controls the drawing process.

2. FUNCTION CONTROL

The function of the machine is determined by the contents of the status word latched in AB, BB with CSR = 0. This word can be read back by the computer except for the MS bit which is replaced by RUN. RUN is high when the brush processor hardware is busy.

F0 – F3 are function bits (see Table 1). S1 and S2 are active low store selects. LUMEN and CHREN are active high enables for writing to luminance and chrominance stores. KSEL is active high and selects extension framestores or brush shape on the brush store. DISCEN enables transfers to or from discs. KINV is active low and is used to invert data on the bypass path of the Brush Processor and also inverts the output of multiplier CB on these cards. KZERO is used to force the output of this multiplier to zero. FCS is active high and enables the fixed colour registers on the Brush Store onto the brush bus.

BCHR (B45) and PLUM (A45) are generated on this card by decoding from the computer bus in LS138 CB and are used to latch pressure data on the Brush Processors.

FUNCTION	
0	Live Video
1	Brush Store Read
2	Brush Store Write
3	Framestore Read
4	Framestore Write
5	Fast Wipe Video
6	Fast Wipe Brush Store
7	Fast Wipe Framestore
8	Draw
9	Draw with Stencil I
10	Draw with Stencil II
11	Copy to Framestore
12	Copy to Brush Store
13	Paste with Stencil I
14	Paste with Stencil II
15	Copy to same Framestore (Invert)

17419, Table 1 Brush Address Card : Function Bits

3. BRUSH STORE CONTROL

The circuitry at the bottom of the circuit diagram is associated with the cycling of the Brush Store. The dynamic memory is continuously refreshed at a rate determined by oscillator HA. Positive edges at HA3 generate a pulse at FG6, which is a request for a brush store cycle, every 10μs. The request is latched at HE5 and passes through HD, after any current cycle is cleared, to be latched at HE9. The signal at TP9 when high selects addresses from the refresh address counter which is internal to the 3242 at AF. At the end of the current cycle (if any) BBUSY goes low allowing the request through HF8 to clock GF3. The resulting transition at GF5 propagates through delay lines GH, HH generating the cycle timing signals at GG and HG outputs. RAS and CAS are buffered out to the Brush Store by AH. CAS is gated off by FG for refresh. Row enable selects row addresses or column addresses from the 3242. LAACH (Look Ahead Address Change) occurs as soon as the CAS address has been latched by the RAMs and is routed by GE6, GE8 to clear the request for the current cycle. This allows addresses to change in advance of the next cycle. CLR clears GF which is set for non-refresh cycles and which is used to route LAACH through GE. The mark-space ratio of HA is such that HA3 pulses low briefly before each request clearing HE via HD1. This prevents the cycle logic locking out if a refresh request does not clear itself with LAACH.

Read or write cycles of the Brush Store are initiated by BSTROBE, TP7. A 30nS request pulse is generated at FG3 and is latched at IE5. The gate at GE1 prevents a race between refresh requests and computer requests. The computer request is serviced in the same way as a refresh request but addresses at the output of 3242 come from inputs A0 - A13. These addresses are generated from a counter chain EC, DC, FC (horizontal) and ED, DD, FD (vertical) which define an array. The complement of the array size is loaded from latches EB, FB, EA, FA and the counters count up until ripple carry at FD15. Ripple carry from FC15 (end of line) enables the vertical chain for one count and reloads the horizontal length via CC6 and FF10. The counters are continuously clocked by PPCK (A36), which comes from the Output Timing card and are synchronously enabled by pulses at TP12 (ADDREN).

Reading or writing of the Brush Store by the computer is carried out by first loading the array size from the computer bus (using BXLEN, BYLEN from CB as strobes) then setting the function and asserting GO. GO is formed from the LS bit of the status word. This sets RUN by causing a load of GD via the synchroniser CD and also loads the counter chain. A BSTROBE is generated by logic array BE for each NDR (for writing) or DTX (for reading) sent by the computer. At the end of each RAM cycle the back edge of BBUSY (TP11), via FH6 and IG4, clocks HB3. HB forms a synchroniser and delivers a pulse and HB9 which is one PPCK wide and which increments the address counter chain. After the correct number of BSTROBES FD15 goes high and enables GD, so RUN is clocked low, ending the sequence. If for some reason RUN is not cleared (e.g. too few strobes) it may be reset by INIT from IA8 which is active for a computer read with CSR = 15.

The 3242 (AF) only handles seven bits of address so the store MS bit is selected by CH. Input A selects row or column and input B selects addresses from latch BD or from shifters DF, DE. This allows the Brush Store to be controlled as one large array or as four blocks. Shifters EF, DF, EE, DE allow the addresses to be bit shifted by up to three bits with lower bits then coming from registers DB (horizontal offset) and DA (vertical offset). The shift factors are latched by BD from the computer bus with BIF from CB.

These shifts and offsets are used to select arrays from different areas of the brush stores.

4. FRAMESTORE ACCESS

The same array counters are used for defining an area when reading from or writing to framestore. The required function bits are loaded and RUN is set by GO. CSTROBE (TP5) is generated by BE for each NDR or DTX. CWRITE is active for writing and drives R/W (A29) and also enables DG3 so that every CSTROBE generates an input enable at B15 which latches input data on the Store card. CSTROBE is also used to generate a request for a computer cycle to the Store Address cards (CREQ, A39). The back edge of CBUSY (TP9) generates ADDREN and increments the counters. The framestore addresses come from the computer address counters on the Store Address cards. These are driven by the 'Address Control Bus' (AB11 - AB15) which consists of the loads and enables from the array counter chain. The store address counters thus run synchronously with the brush address counters. The address control bus is driven by tri-state buffers AH, BH. When live video input is selected, SELVIDEO turns off the drives and the Input Timing card is enabled via B14 and drives the bus. For reading data from disc to framestore the bus is driven by the Size card. In this case CEN and CIPEN are still required and are driven by DH. The array counters are still used to provide EARLY EVEN, A27 and LINE CLOCK, B30 and are incremented by BADCK, B27 which is selected by IG. YDIS, A30 disables the vertical counters for the first three lines to allow for data delays through the Filter card.

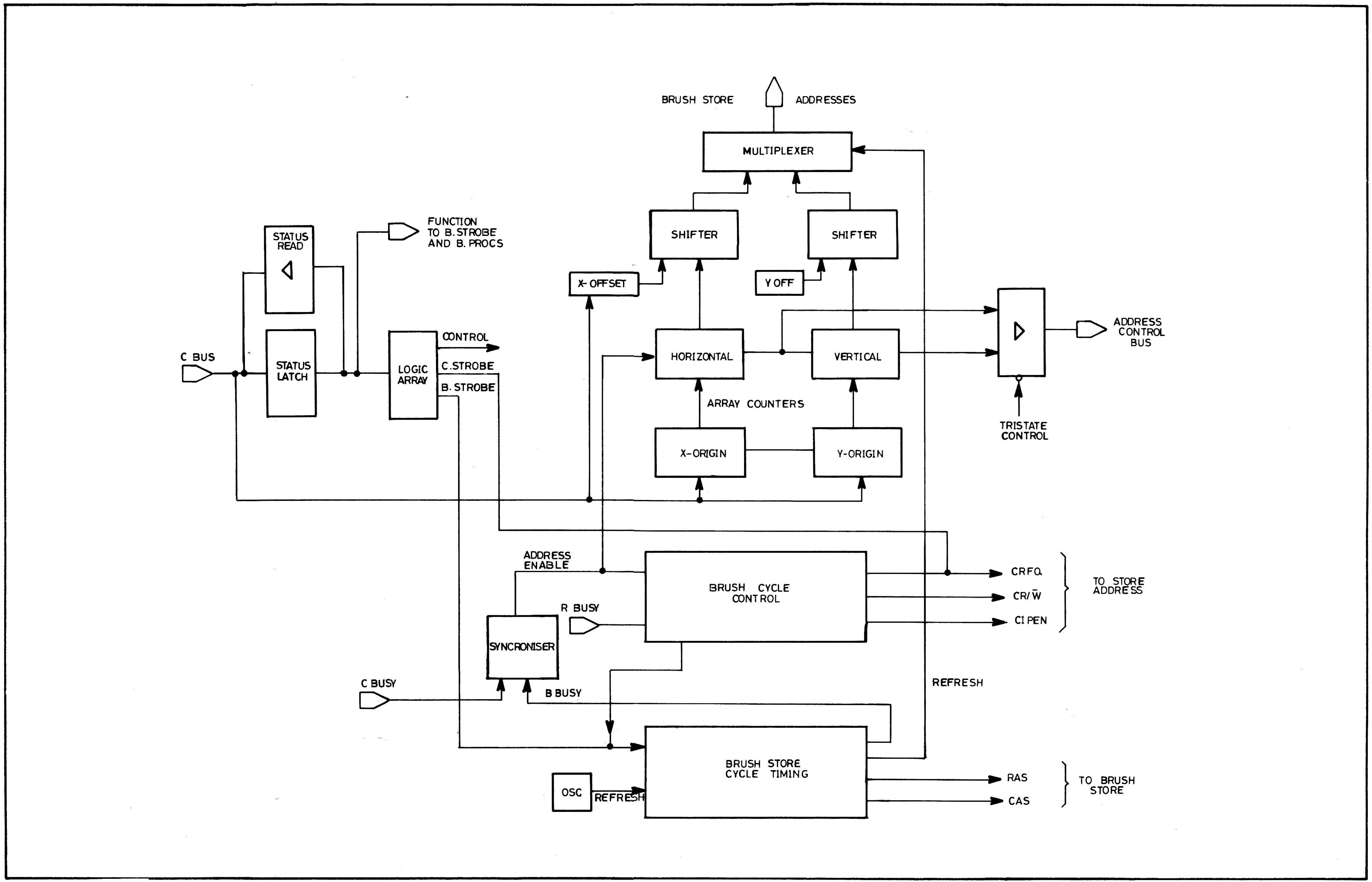
5. DRAWING

The drawing process consists of a read modify write on an array of the framestore. The size of which is loaded in the brush address counters. The function bits are set as required and a GO pulse starts off the process. RUN is set. PROCEN goes high and a series of processor cycles are executed, one for each pixel. PROCEN active at HC12 causes CYCLE (TP10) to go high after two RBUSY pulses at HC11. GB is cleared to the READ state and the edge of CYCLE gives a pulse at DG8 which generates CREQ via FH12 and also a Brush Store request at FF12. The resulting framestore read and brush store read cycles present data to the inputs of the Brush Processor card. The back edge of BBUSY or CBUSY, whichever is later at FH6, clocks HB3 and GB3. Data at HB2 is low at this point so there is no change at HB5 but CB5 changes from READ to WRITE. The R/W edge is turned into a pulse by GC which is synchronous to PFLAG and therefore to computer read data from the framestore. This is delayed in EG to allow for data to propagate through the brush processor and then generates a CREQ for the store write. At the end of this, CBUSY again clocks 3HB and 3GB but this time HB2 is high and an ADDREN pulse is generated which increments the counters. CYCLE is cleared via HC1 and GB5 resets to READ. The next RBUSY starts another cycle. This sequence repeats for each pixel until FD15 resets RUN.

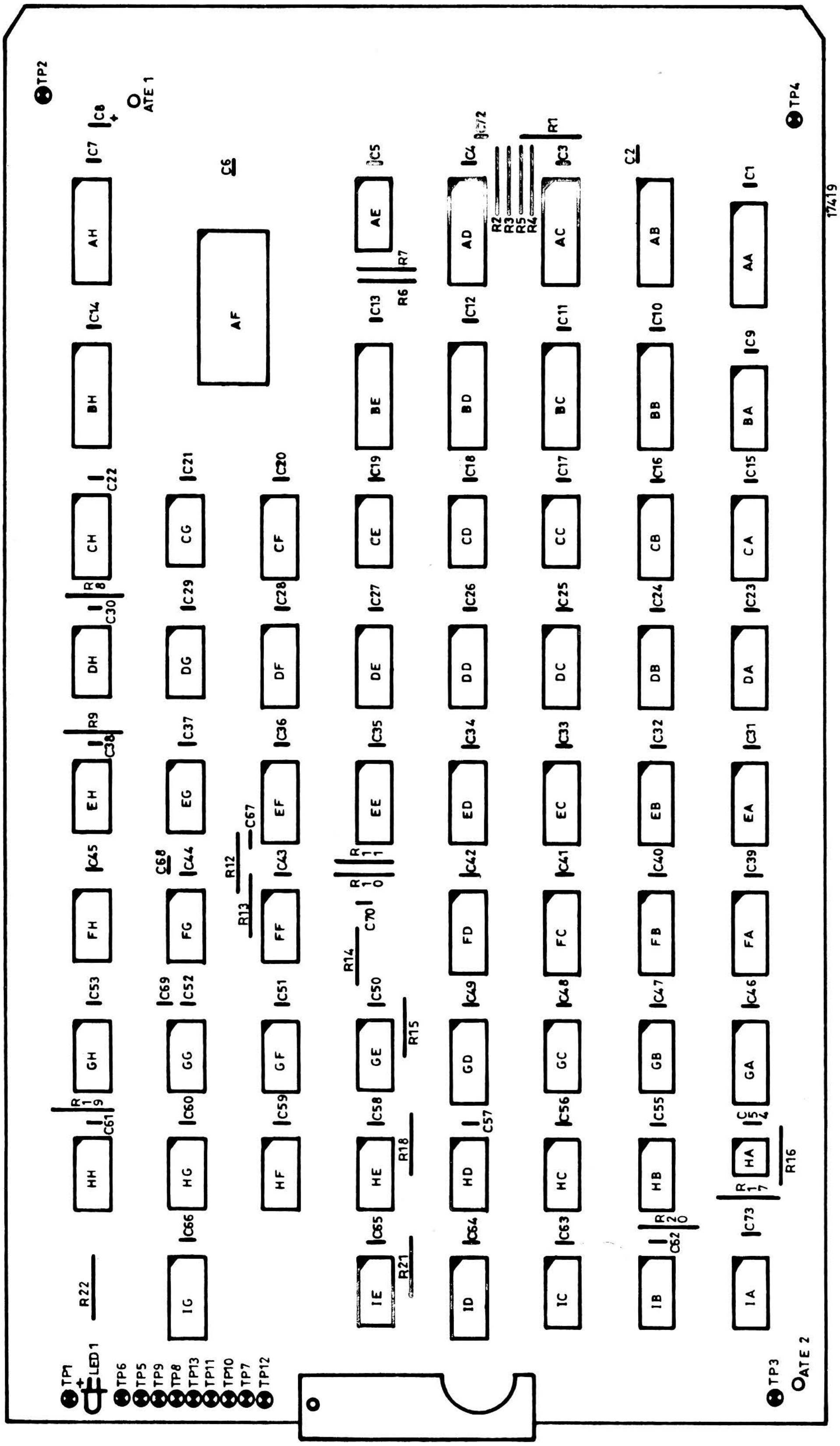
Selector ID modifies the cycle for function 12 to provide a framestore read followed by a brush store write to enable a copy of framestore to brush store.

REF.	DESCRIPTION	STOCK CODE
CAPACITORS		
C1-C66	100000pF, 50V, +80%-20%	03/06/0233
C67	270pF, 100V, 10%	03/06/0349
C68	82pF, 100V, 20%	03/06/0624
C69	180pF, 100V, 10%	03/06/039X
C70	100pF, 100V, 10%	03/06/0306
C71	1000pF, 100V, 10%	03/06/0314
C72, C73	150pF, 100V, 10%	03/06/0365
RESISTORS		
R1-R3	470Ω, 250mW, 2%, 100ppm	01/01/0557
R4, R5	1kΩ, 250mW, 2%, 100ppm	01/01/0646
R6-R11	470Ω, 250mW, 2%, 100ppm	01/01/0557
R12	270Ω, 250mW, 2%, 100ppm	01/01/0476
R13	200Ω, 250mW, 2%, 100ppm	01/01/0425
R14	220Ω, 250mW, 2%, 100ppm	01/01/0441
R15	200Ω, 250mW, 2%, 100ppm	01/01/0425
R16	22kΩ, 250mW, 2%, 100ppm	01/01/1014
R17	470Ω, 250mW, 2%, 100ppm	01/01/0557
R18	2.2kΩ, 250mW, 2%, 100ppm	01/01/1642
R19, R20	1kΩ, 250mW, 2%, 100ppm	01/01/0646
R21	2.2kΩ, 250mW, 2%, 100ppm	01/01/1642
R22	390Ω, 250mW, 2%, 100ppm	01/01/053Y
INTEGRATED CIRCUITS		
AA	74LS244N	04/01/2828
AB	74LS373N	04/01/3921
AC	74LS244N	04/01/2828
AD	74LS240N	04/01/2879
AE	74LS14N	04/01/3425
AF	Dil Switch	04/03/1709
AH	74S240N	04/01/3786
BA	74LS244N	04/01/2828
BB	74LS373N	04/01/3921
BC	74LS244N	04/01/2828
INTEGRATED CIRCUITS (Cont.)		
BD	74LS374N	04/01/3328
BE	Programme set make from the fo'ling (Ref. only) 1 x 04/01/541X 16L8CN	
BH	74S241N	04/01/3794
CA, CB	74LS138N	04/01/109Y
CC	74LS08N	04/01/417Y
CD	74LS74N	04/01/0728
CE	74LS00N	04/01/006X
CF	74LS157N	04/01/1236
CG	74LS02N	04/01/1724
CH	74LS153N	04/01/118X
DA, DB	74LS174N	04/01/1422
DC, DD	74LS163N	04/01/1317
DE, DF	25S10PC	04/01/8583
DG	74LS08N	04/01/417Y
DH	74LS125N	04/01/3603
EA, EB	74LS174N	04/01/1422
EC, ED	74LS163N	04/01/1317
EE, EF	25S10PC	04/01/8583
EG	74LS164N	04/01/3719
EH	74LS05N	04/01/4758
FA, FB	74LS174N	04/01/1422
FC, FD	74LS163N	04/01/1317
FF	74LS02N	04/01/1724
FG	74LS08N	04/01/417Y
FH	74LS27N	04/01/3484
GA	74S133N	04/01/3638
GB, GC	74LS74N	04/01/0728
GD	74LS163N	04/01/1317
GE	74LS00N	04/01/006X
GF	74LS74N	04/01/0728
GG	74S86N	04/01/0825
GH	Delay Line	30/01/028Y
HA	Dil Switch	04/01/2224
HB, HC	74LS74N	04/01/0728
HD	74LS08N	04/01/417Y
HE	74S74N	04/01/0698
HF	74LS00N	04/01/006X
HG	74S86N	04/01/0825
HH	Delay Line	
IA	74LS30N	04/01/0469
IB	74LS32N	
IC	74S74N	04/01/0698
ID	74LS157N	04/01/1236
MISCELLANEOUS		
LED1	Light Emitting Diode Green	06/03/0033

17419 Component List



17419, Figure 1 Brush Address Card Block Diagram


TP1
TP2
TP3
TP4
TP5
TP6
TP7
TP8
TP9
TP10
TP11
TP12
TP13
LED 1
ATE 1
ATE 2
17419
AA
AB
AC
AD
AE
AF
AH
BA
BB
BC
BD
BE
BH
CA
CB
CC
CD
CE
CF
CG
CH
DA
DB
DC
DD
DE
DF
DG
DH
EA
EB
EC
ED
EE
EF
EG
EH
FA
FB
FC
FD
FF
FG
FH
GA
GB
GC
GD
GE
GF
GG
GH
HA
HB
HC
HD
HE
HF
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IA
IB
IC
ID
IE
IG
C1
C2
C3
C4
C5
C6
C7
C8
C9
C10
C11
C12
C13
C14
C15
C16
C17
C18
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C20
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C57
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C59
C60
C61
C62
C63
C64
C65
C66
C67
C68
C69
C70
C73
R1
R2
R3
R4
R5
R6
R7
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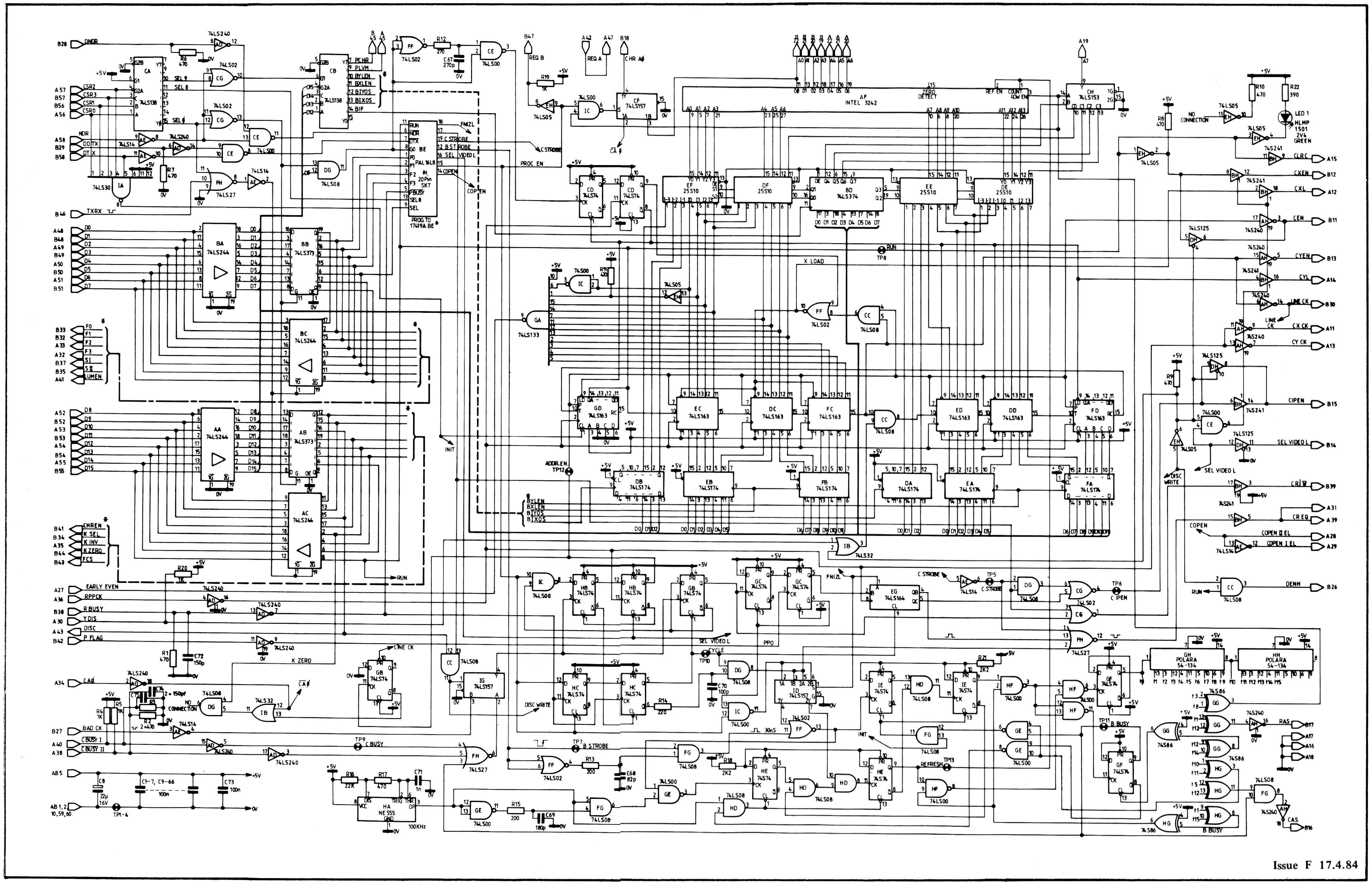
R18
R19
R20
R21
R22



Issue F 17.4.84

17419, Figure 2 Brush Address Card : Circuit Diagram and Component Layout

BRUSH STORE CARD

17421

1. INTRODUCTION

The Brush Store card contains three sections of dynamic RAM storage for the brush, the data interface between the System Bus and the Brush Data Bus, and the registers used to provide fixed colours along the Brush Data Bus to the rest of the system.

2. CIRCUIT DESCRIPTION

The Brush Address provides the multiplexed address, RAS and CAS for the Brush RAMs. These signals are buffered by 74LS244's CE and DE before being passed to the RAM chips. The Brush Address also handles refresh requirements for these RAMs.

The Brush storage consists of twenty-four 64k RAM chips which are divided to form three sections each 8-bits deep. These sections are used for luminance, chrominance, and extension respectively. The chrominance store contains alternate B-Y and R-Y which may on occasions need to read out in the opposite order. To facilitate this the least significant bit of the chrominance address is fed in separately from the Brush Address.

When reading the Brush Store the RAM outputs are latched in 74LS374s DB, DD, DC by the signal BCK. Since the data is stable by the end of the CAS cycle the inverse of this signal is used to generate BCK. When enabled the latched data is passed onto the Brush Data Bus for use by the Brush Processor or via tri-state buffers to the system bus for transfer to the control computer or the Disc Data Buffer.

Similarly, data for writing into the Brush Store is obtained from the Brush Data Bus and may have come from the Brush Processor, the Filter (from the disc), or the System Bus via transparent latches AC, AB, BB. When these latches are holding data they provide a fixed colour on the Brush Data Bus for filling the Brush Store or Framestores (via the Brush Processor) with a constant colour.

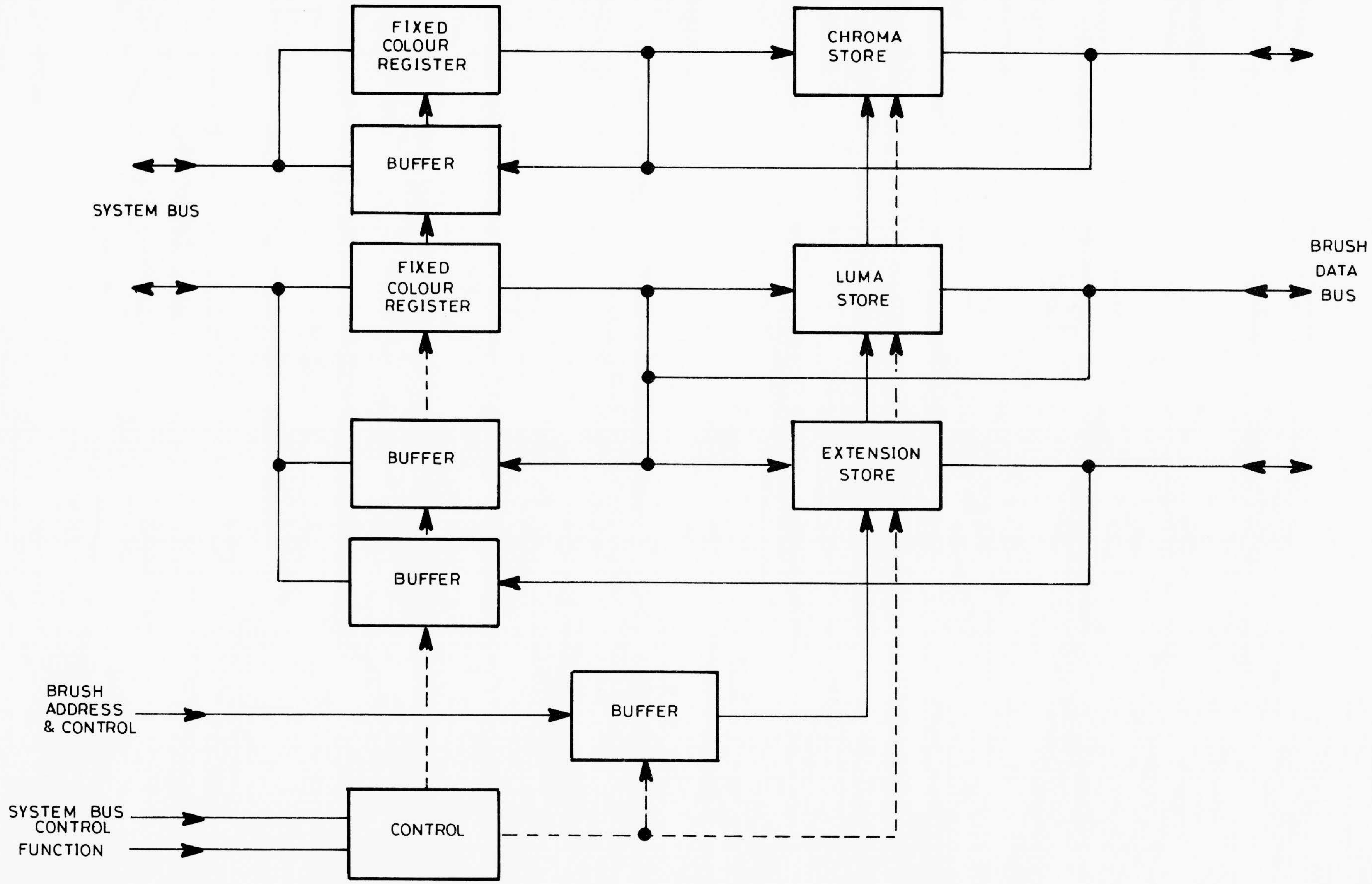
Data is transferred between the System Bus and the Brush Data Bus when the System Bus CSR code is eight. This is decoded by AA and BC together with SYSTEM BUS CONTROL signals TX/RX and NDR to provide the transparent latch enables (AC, AB, BB) and tri-state buffer enables (CB, CD, CC) appropriately. The tri-state buffer enables are further gated with luminance, chrominance and extension enables by chip BD depending on the function chosen by the computer.

Which data is tri-stated onto which Bus at any particular time is determined by the function (F3, F2, F1, F4) and other bits of the system status word, FCS (Fixed Colour Select) and KSEC (Extension Select). These are decoded by PROM AD to provide various output enable signals to data chips on the card. The PROM assumes that the system computer is in charge of the buses. Should Filter or Tape cards wish to use the bus then they may override the normal PROM signals by lowering BBUSA (Brush Data Bus Available).

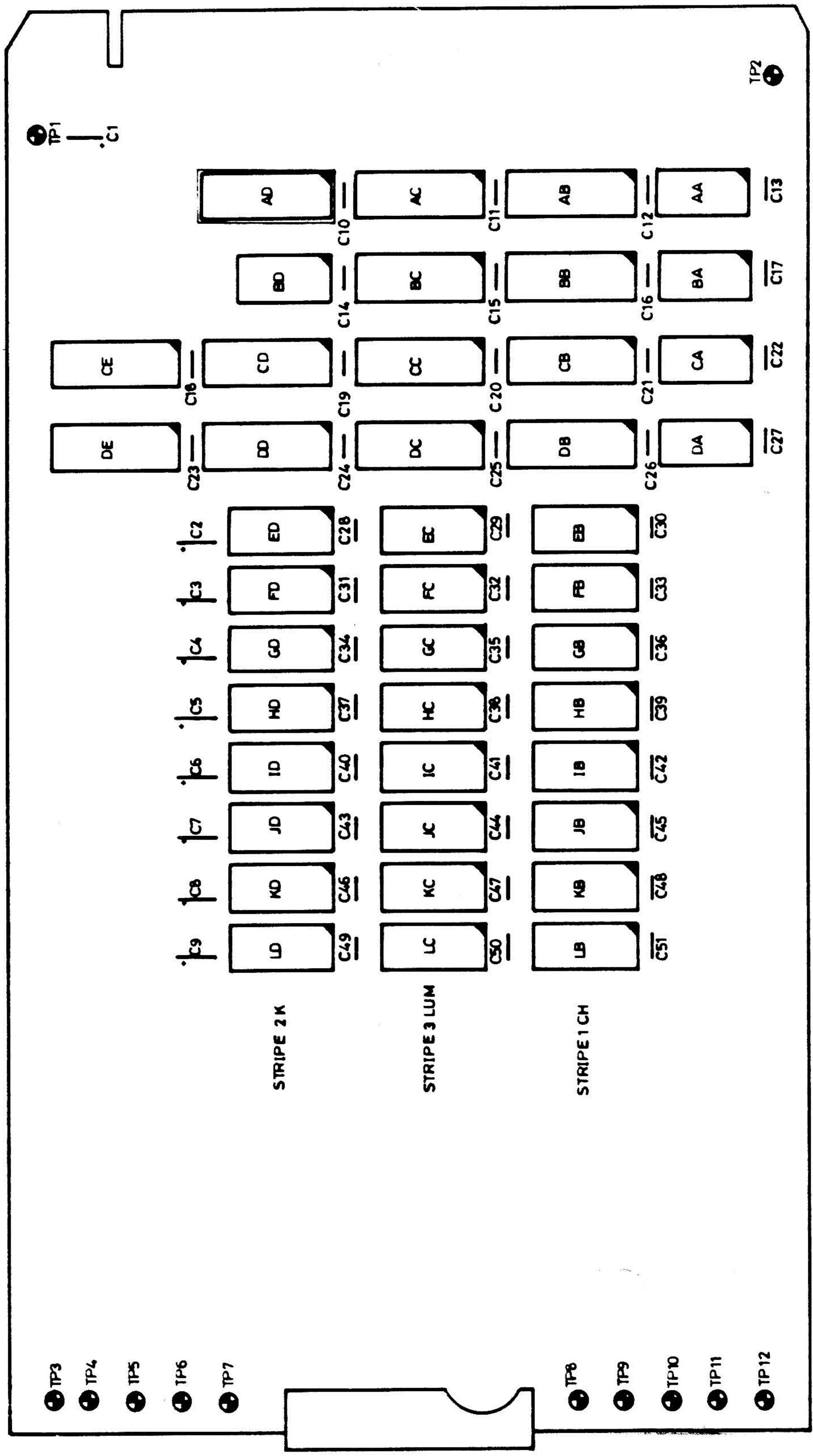
When the fixed colour latches are being used they need to generate alternating B-Y and R-Y on the chrominance data bus. This is accomplished by picking up the framestore least significant address bit CA0 (Computer Address bit 0) and using it via BD and DA to alternating output enable latch chips AB and BB.

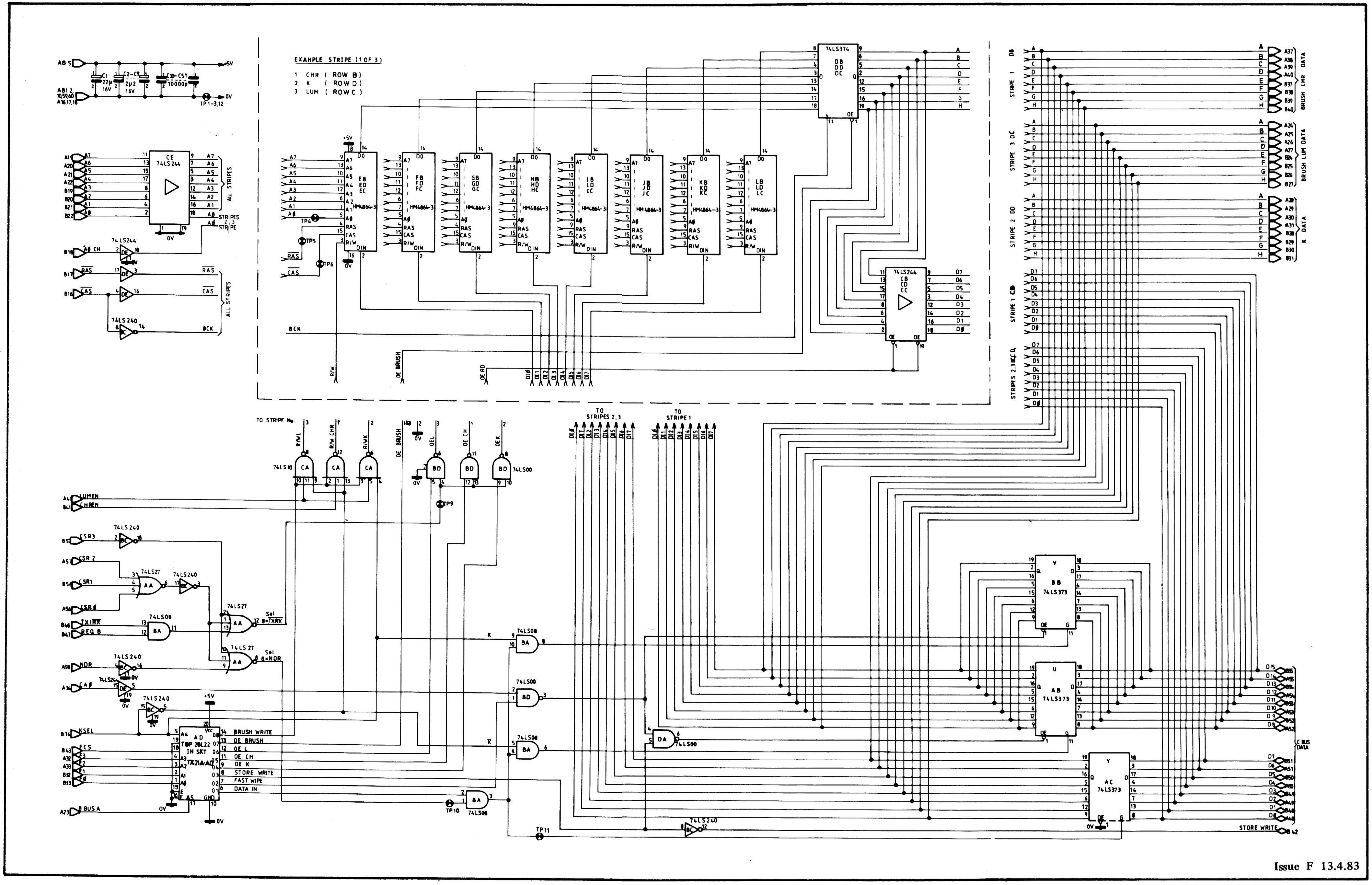
REF.	DESCRIPTION	STOCK CODE
CAPACITORS		
C1	22μF, 16V, 20%	03/03/0253
C2-C9	2.2μF, 16V, 20%	03/03/0067
C10-C51	10000pF, 100V, +80%-20%	03/06/0101
INTEGRATED CIRCUITS		
AA	74LS27N	04/01/3484
AB, AC	74LS373N	04/01/3921
AD	Programmed set make from 1 x 04/01/3107-28L22	
BA	74LS08N	04/01/417Y
BB	74LS373N	04/01/3921
BC	74LS240N	04/01/2879
BD	74LS00N	04/01/006X
CA	74LS10N	04/01/3132
CB-CE	74LS244N	04/01/2828
DA	74LS00N	04/01/006X
DB-DD	74LS374N	04/01/3328
DE	74LS244N	04/01/2828
EB-LD	Dil Switch	04/03/3353

17421 Component List



17421, Figure 1 Brush Store Card Block Diagram


TP1
C1
TP2
17421
AD
AC
AB
AA
C10
C11
C12
C13
BD
BC
BB
BA
C14
C15
C16
C17
CE
CD
CC
CB
CA
C18
C19
C20
C21
C22
DE
DD
DC
DB
DA
C23
C24
C25
C26
C27
C2
ED
C28
EC
C29
EB
C30
C3
FD
C31
FC
C32
FB
C33
C4
GD
C34
GC
C35
GB
C36
C5
HD
C37
HC
C38
HB
C39
C6
ID
C40
IC
C41
IB
C42
C7
JD
C43
JC
C44
JB
C45
C8
KD
C46
KC
C47
KB
C48
C9
LD
C49
LC
C50
LB
C51
STRIPE 2 K
STRIPE 3 LUM
STRIPE 1 CH
TP3
TP4
TP5
TP6
TP7
TP8
TP9
TP10
TP11
TP 12



Issue F 13.4.83

17421, Figure 2 Brush Store Card : Circuit Diagram and Component Layout

BRUSH PROCESSOR CARD

17593

1. INTRODUCTION

Two Brush Processors are used in the system, one for luminance and one for chrominance. They are identical and may be freely interchanged. This card takes data from several sources, Framestore, Brushstore, Framestore Extension, Brushstore Extension and Pressure, and combines them in various possible mathematical ways to produce an answer for feeding back to the framestore.

2. CIRCUIT DESCRIPTION

Data from the framestore via buffer AG and data from the Brush data bus are compared by the 74S85s DG, EF and subtracted by the ALUs FE, CE to form a sign and magnitude answer to multiplier DD. Here the difference signal is multiplied by a factor derived from Store Extension, Brush Extension and Pressure to produce a 16-bit number for adding to the original framestore data by ALUs FB, FC, FE, FD. If the sign of the difference signal is negative, then the ALUs perform a subtraction instead of an addition of the difference magnitude.

If 8-bit only processing is being performed then the data from FE, FD is fed via selectors GB, GC to the lower framestore for optionally writing to that store.

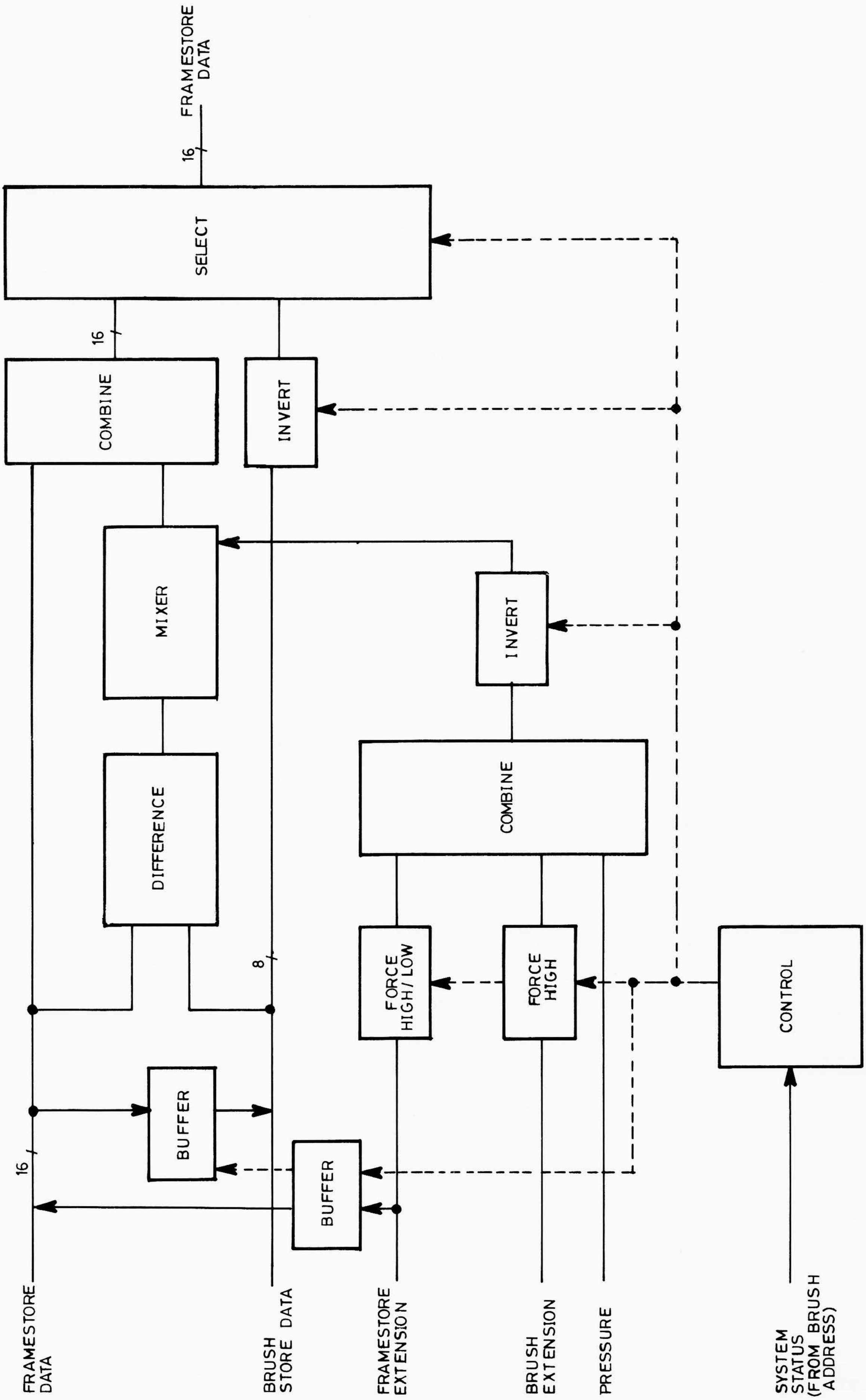
Pressure is stored inside multiplier BB when commanded to do so by signal PCK (Pressure Clock). Here it is multiplied by Brush Extension data, or 255 if latch AD is disabled, and passed on to CB. This multiplier further combines it with data from one of the framestore extensions, or 255, or 0 depending on the state of selectors CA, DA. Finally, the data is optionally inverted before being passed to multiplier EB whose usage is described above.

Various bypass paths are provided on the card. Data from the Brush Data Bus may completely bypass the processing via optional inverters and selectors GE, GD for transfer directly to the framestore. Data from the framestore extension may be processed in place of framestore picture data by enabling buffer AF or taken from there to the Brush Data Bus via buffer CF. Data from the lower framestore may also be taken to the Brush Data Bus via buffer DF for sending back to the System Bus or onwards to the upper framestore.

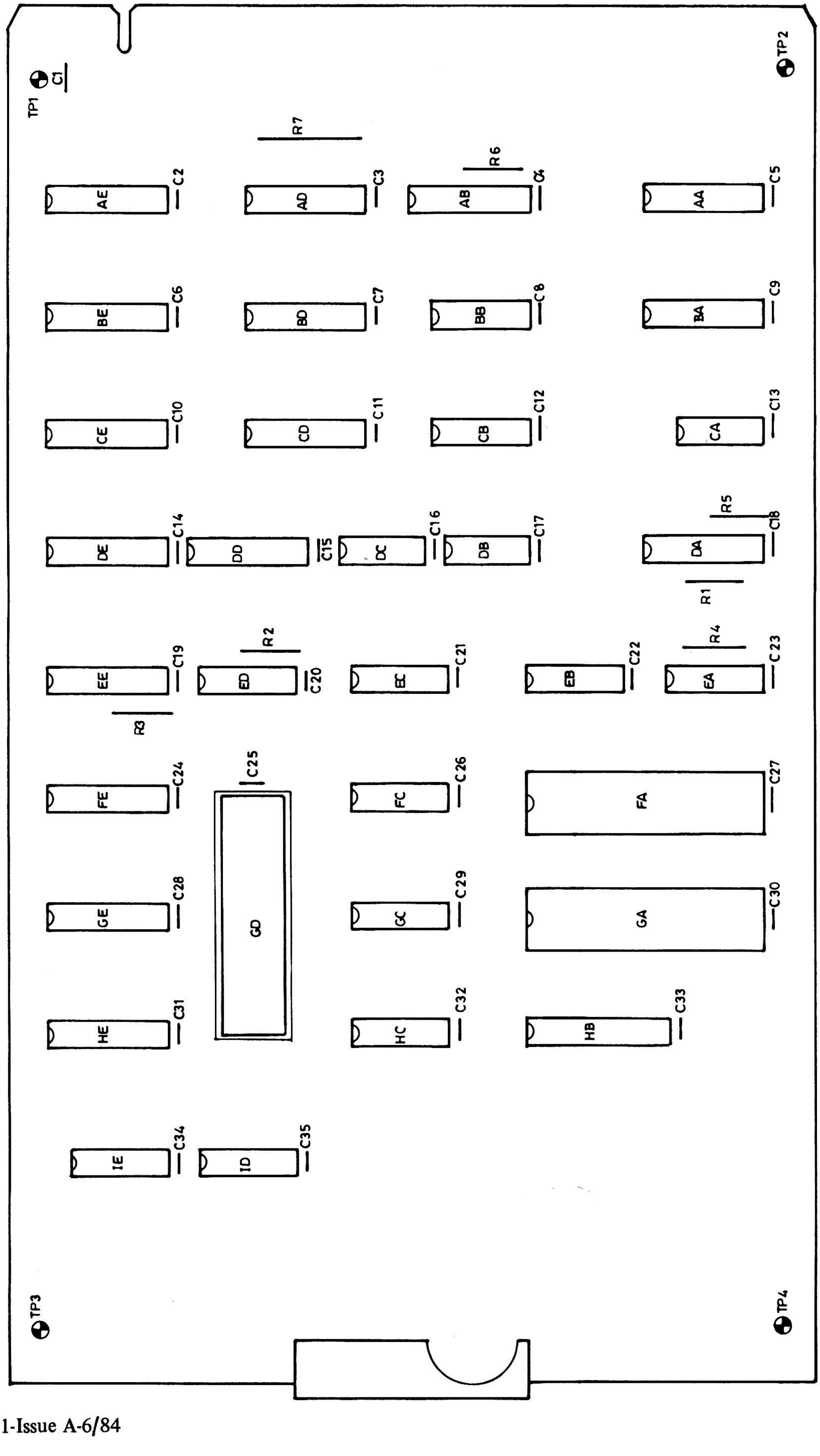
The various permutations of data paths on this card are controlled by the function and other bits of the system status word (see Brush Address). PROM AB is used to decode these signals and provides the buffer output enables and other control signals for the card. This PROM also listens to BBUSA (Brush Data Bus Available) and disables the data buffers if any other card demands the Brush Data Bus.

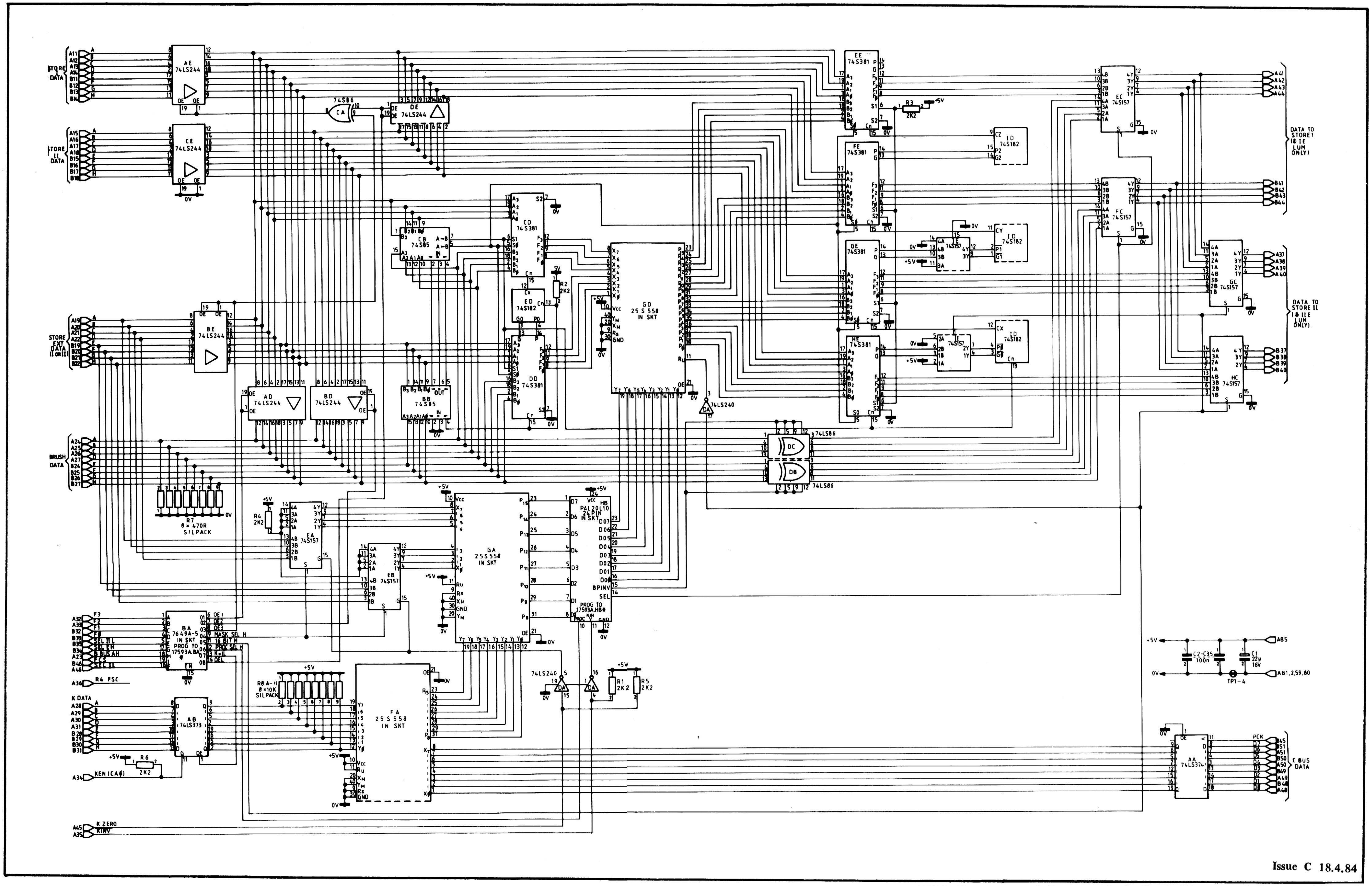
REF.	DESCRIPTION	STOCK CODE
CAPACITORS		
C1	22µF, 16V, 20%	03/03/0253
C2-C35	100000pF, 50V, +80%-20%	03/06/0233
RESISTORS		
R1-R6	2.2kΩ, 250mW, 1%,	01/01/0727
R7	470Ω x 8, 125mW, 5%, 300ppm	01/08/052Y
R8	10kΩ x 8, 125mW, 5%, 300ppm	01/08/0555
INTEGRATED CIRCUITS		
AA	74LS374N	04/01/3328
AB	74LS373N	04/01/3921
AD, AE	74LA244N	04/01/2828
BB	74S85N	04/01/0809
BD, BE	74LS244N	04/01/2828
CA	74LS86N	04/01/0833
CB	74S85N	04/01/0809
CD	74S381N	04/01/4308
CE	74LS244N	04/01/2828
DA	74LS240N	04/01/2879
DB, DC	74LS86N	04/01/0833
DD	74S381N	04/01/4308
DE	74LS244N	04/01/2828
EA-EC	74S157N	04/01/121X
ED	74S182N	04/01/3735
EE	74S381N	04/01/4308
FA	25S558PC	04/01/6602
FC	74S157N	04/01/121X
FE	74S381N	04/01/4308
GA	25S558PC	04/01/6602
GC	74S157N	04/01/121X
GE	74S381N	04/01/4308
HC	74S157N	04/01/121X
HE	74S381N	04/01/4308
ID	74S182N	04/01/3735
IE	74S157N	04/01/121X

17593 Component List



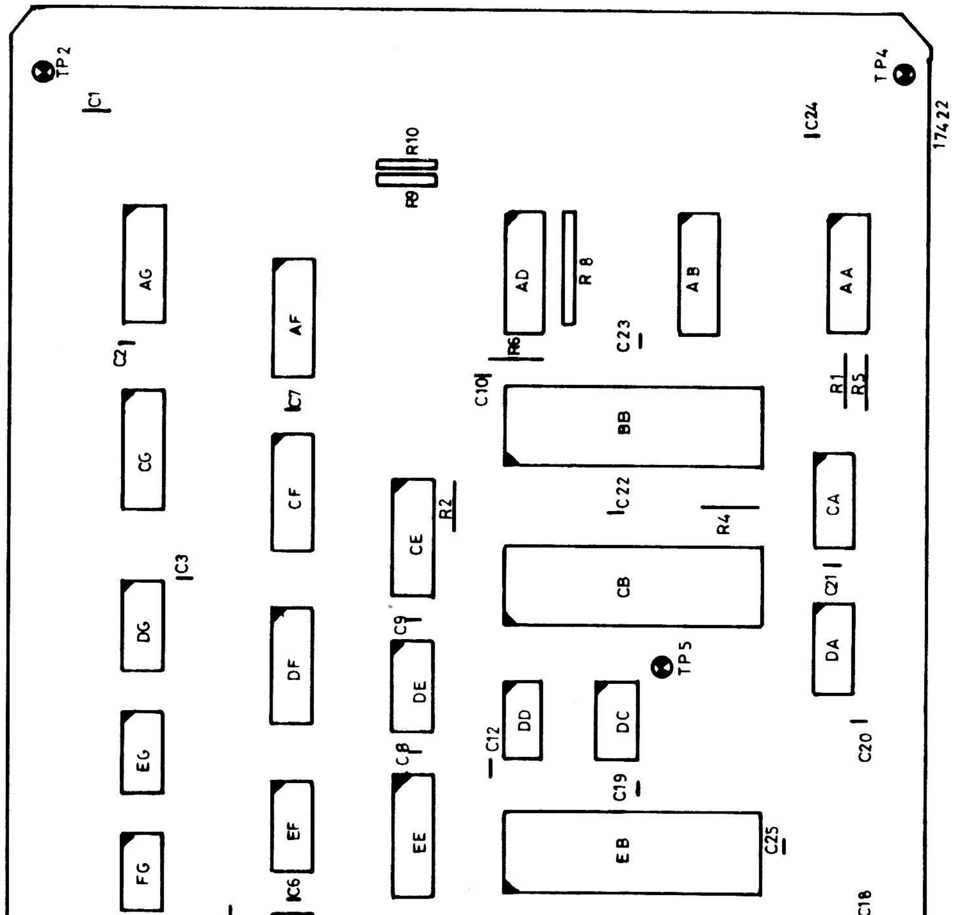
17593, Figure 1 Brush Processor Card Block Diagram

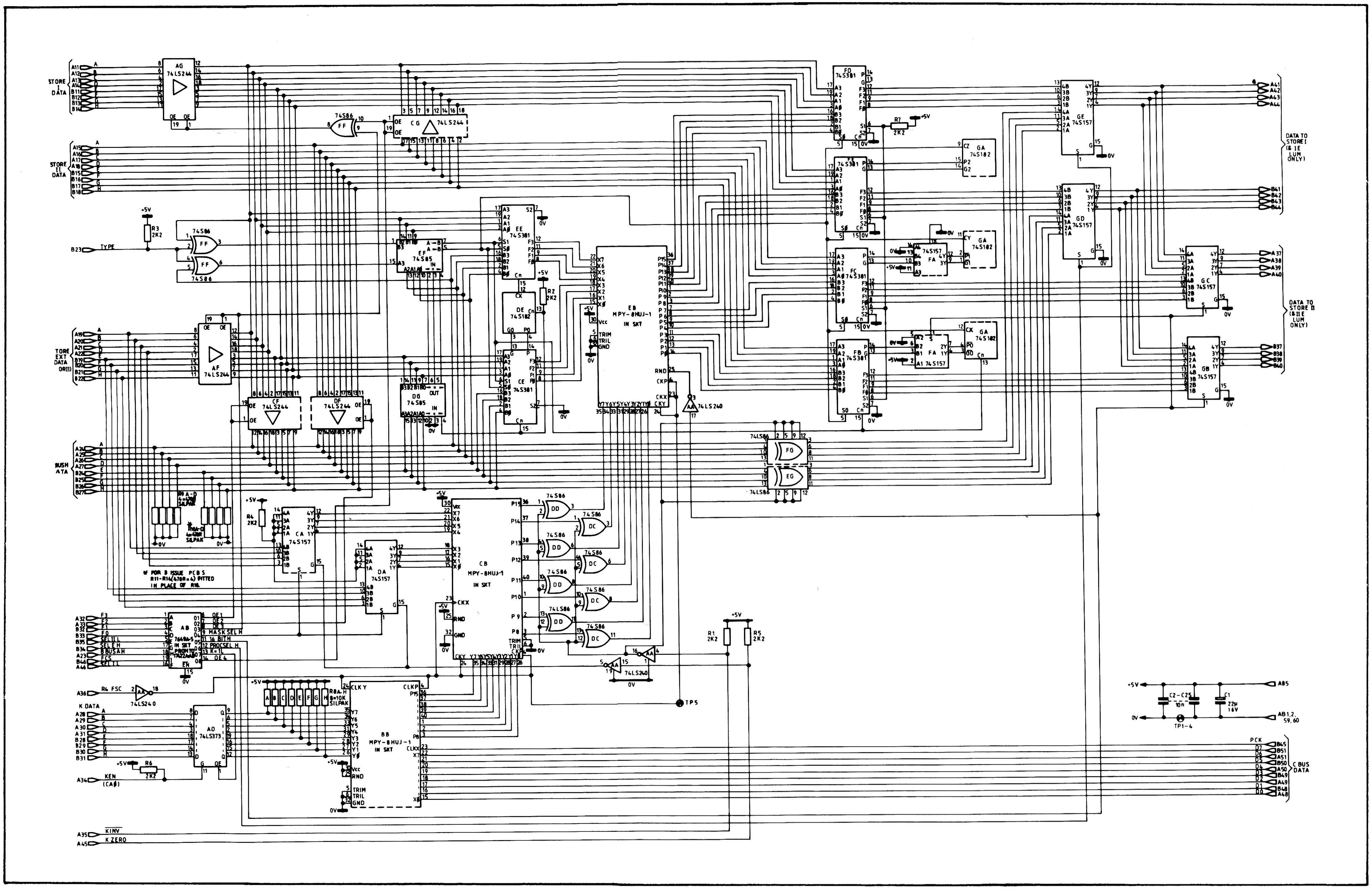

TP1
C1
TP2
17593
R7
R6
AE
C2
AD
C3
AB
C4
AA
C5
BE
C6
BD
C7
BB
C8
BA
C9
CE
C10
CD
C11
CB
C12
CA
C13
R5
DE
C14
DD
C15
DC
C16
DB
C17
DA
C18
R1
R2
R4
EE
C19
ED
C20
EC
C21
EB
C22
EA
C23
R3
C25
FE
C24
FC
C26
FA
C27
GD
GE
C28
GC
C29
GA
C30
HE
C31
HC
C32
HB
C33
IE
C34
ID
C35
TP3
TP4



Issue C 18.4.84

17593, Figure 2 Brush Processor Card : Circuit Diagram and Component Layout


TP2
C1
R10
R9
C24
TP4
17422
AG
AF
AD
R8
AB
AA
C2
C23
R6
C10
BB
R1
R5
C7
CG
CF
C22
CA
R2
R4
CE
C3
CB
C21
DG
C9
DF
DE
TP5
DA
DD
DC
C12
C8
EG
C20
C19
EF
EE
EB
C25
FG
C6
C18
R3
FF
C4
C5
FE
FD
FC
FB
FA
R7
C11
C13
C14
C15
C16
C17
GE
GD
GC
GB
GA
TP
TP3



17422, Figure 3, Brush Processor Card : Circuit Diagram and Component Layout

INPUT TIMING CARD

17447

1. INTRODUCTION

This card is used only for live video input and is enabled when video input is selected by the artist. The computer sets function zero in the status word on the Brush Address card and causes SELVIDEO to be asserted (active low at edge connector B14). This allows signals from the card to drive the 'address control bus' AB11 - AB16 and enables video data onto the 'brush bus', AB19 - AB27. The data originates on the ADC card and consists of eight bits of luminance and eight bits of chrominance, which are alternately R-Y and B-Y. The data is driven at ECL levels between the lower and upper backplanes and is reconverted to TTL by BC, BD, AC, AD. The ADC sample clocks and chroma multiplex clock are provided from here and are again ECL driven by BB.

2. CIRCUIT DESCRIPTION

The card receives mixed syncs (TP6) from the Input Locking card. The input source is selected on the Locking card under the control of this card via VTR B47 and RGB A47. Latch AB holds a control word loaded by NDR from the computer with CSR = 4. Bit 1 selects encoded source when high and RGB source when low. Bit 2 selects the digital transfer input as source. This is active high and overrides bit 1. Bit 3 will force MONO. Bit 0 forces data into one field of the framestore only.

From mixed syncs monostables EB generate a line pulse, the first half of EB being a half-line lockout. Monostables EA allow independent horizontal position adjustment for RGB and coded sources. Only one half is active the other being held clear by bit 1 of the control word. Oscillator DA drives a counter chain EF, EE, ED which is locked to the line pulse. The high to low transition at pin 4 of DG, from the most significant output of the counter, is driven into coincidence with the line pulse on pin 10 of CB. CB and C3 form a sample and hold driving error amplifier CA which controls the oscillator frequency by changing the capacitance of varicap diode D1. The counter chain outputs are used by PROM EG to generate horizontal timing signals.

Monostable FB generates a vertical reset pulse for vertical synchronisation. Capacitor C10 charges up during low going line sync pulses but only charges sufficiently to trigger pin 2 of FB during the broad pulses of the field group. Counter chain FF, FE, FD is clocked by a half line clock from the horizontal PROM via latch EH. This counter chain is used to generate vertical timing signals in PROM FG.

Vertical and horizontal signals are combined in PROM DH to generate the address control signals required to drive the counters on the Store Address card.

WXL	is a horizontal reset.
WYLD	is a vertical reset.
WXEN	enables horizontal counter during picture.
WYEN	enables vertical counters during pictures.
WEN	is a static overall enable.
WPPCK	is horizontal picture point clock.
WPEN	loads data into the framestores.
BG B18	Burst Gate used by the chroma separator.

Field blanking is used to drive REQB (open collector) to the computer and is active during picture. The computer cannot send commands when REQB is active and waits for REQB to become inactive before freezing the input.

To compensate for relative analogue delays of chrominance in the chroma separator and ADC cards there is a digital delay in the luminance data path. This is done by RAMs CD and CC and address counter DC. The amount of delay is set by wire links. The delay is disabled by the clear pin 1 of DC when RGB is selected.

When MONO is selected AG drives the chroma bus with 128, equivalent to no chroma.

When FCS B23 is active the data bus drivers are disabled. This allows the fixed colour registers on the Brush Store card to drive the bus filling the store with fixed colour at video rate.

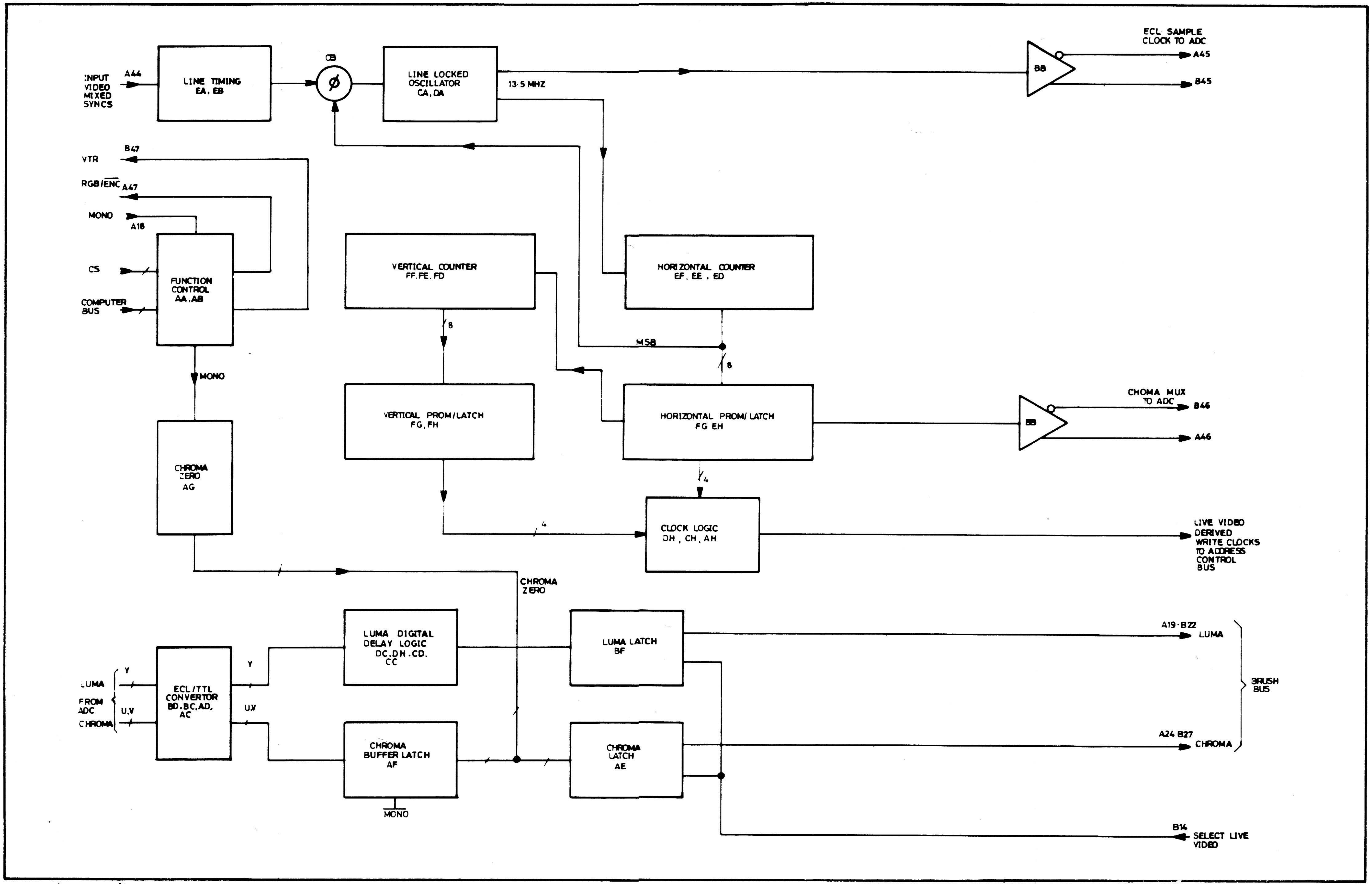
The card has a link (LK1) which sets the counter load values for NTSC or PAL standards. Different PROMs and crystal oscillators are required for the two standards.

Normal link positions are:

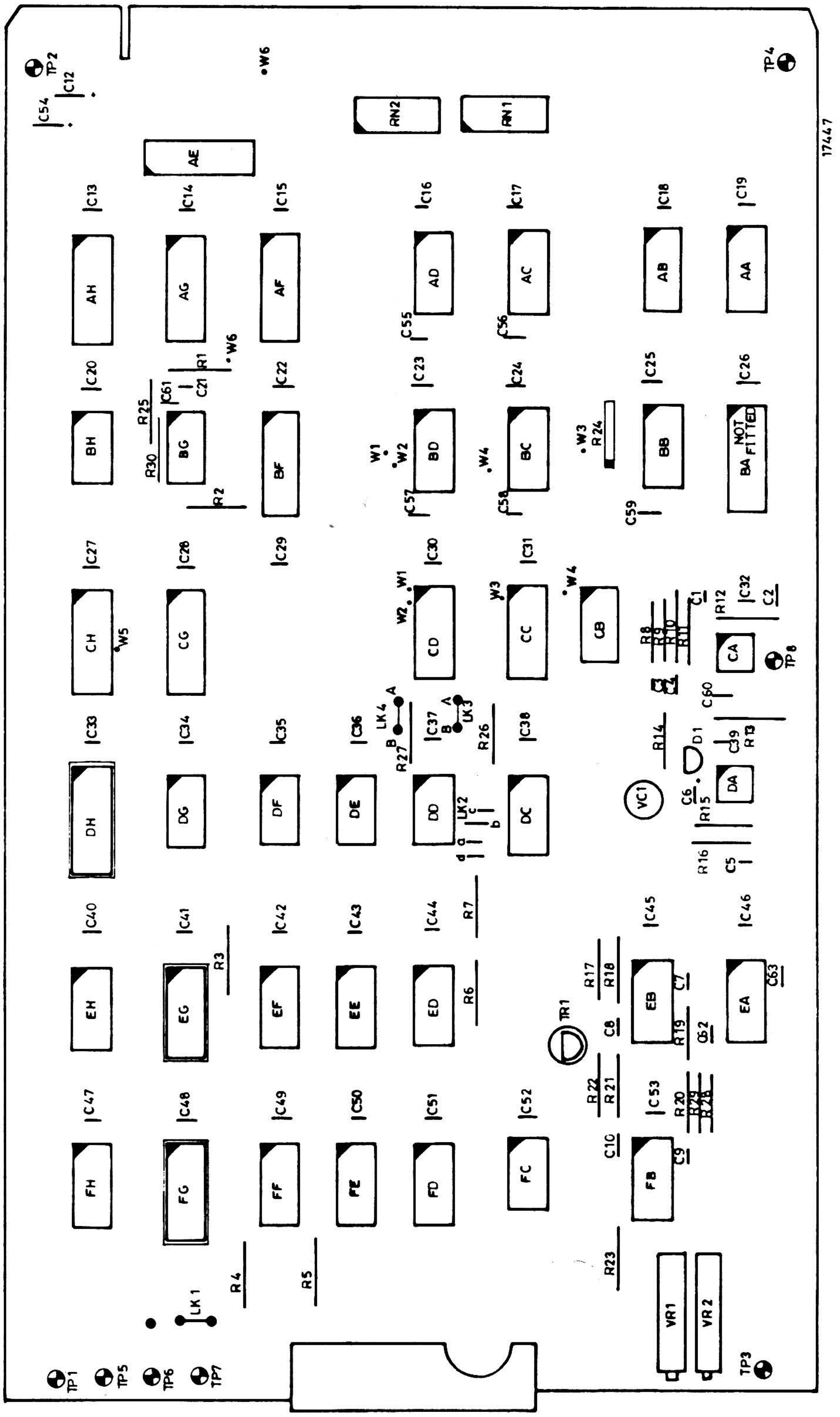
		NTSC	**PAL**
LK2	DC pin 3	1	0
	DC pin 4	0	0
	DC pin 5	0	1
	DC pin 6	0	1
LK1		525	625
LK3	SHORTED		
LK4	SHORTED		

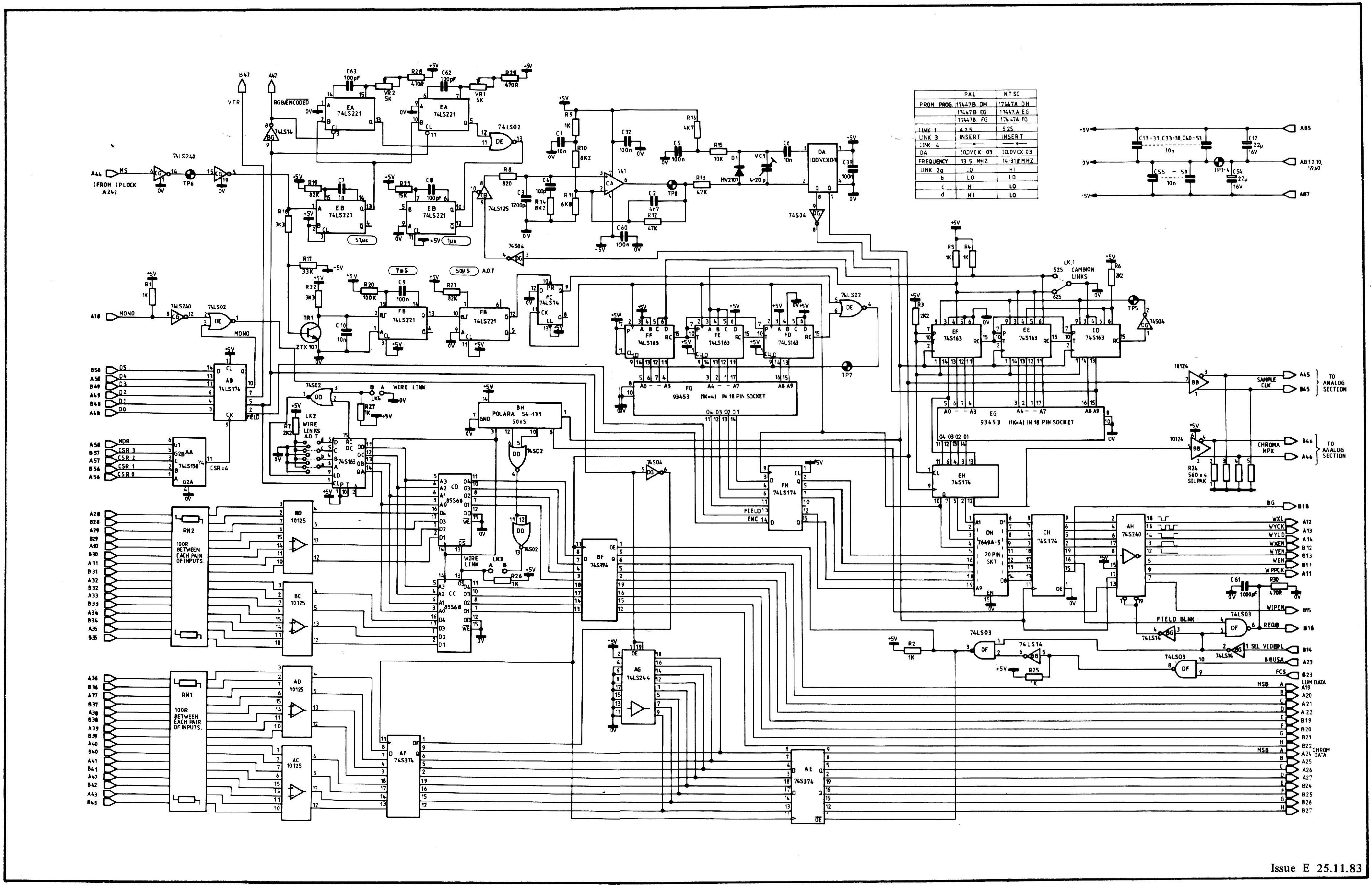
REF.	DESCRIPTION	STOCK CODE
CAPACITORS		
C1	10000pF, 100V, +80%-20%	03/06/0101
C2	4700pF, 100V, +80%-20%	03/06/008X
C3	1200pF, 100V, 10%	03/06/050Y
C4	100pF, 100V, 10%	03/06/0306
C5	100000pF, 50V, +80%-20%	03/06/0233
C6	10000pF, 100V, +80%-20%	03/06/0101
C7	1000pF, 100V, 10%	03/06/0314
C8	100pF, 100V, 10%	03/06/050Y
C9	100000pF, 50V, +80%-20%	03/06/0233
C10	10000pF, 100V, +80%-20%	03/06/0101
C11	1000pF, 100V, 10%	03/06/0314
C12	22μF, 16V, 20%	03/03/0253
C13-C31	10000pF, 100V, +80%-20%	03/06/0101
C32	100000pF, 50V, +80%-20%	03/06/0233
C33-C38	10000pF, 100V, +80%-20%	03/06/0101
C39	100000pF, 50V, +80%-20%	03/06/0233
C40-C53	10000pF, 100V, +80%-20%	03/06/0101
C54	22μF, 16V, 20%	03/03/0253
C55-C59	10000pF, 100V, +80%-20%	03/06/0101
C60	100000pF, 50V, +80%-20%	03/06/0233
C61	1000pF, 100V, 10%	03/06/0314
C62, C63	100pF, 100V, 10%	03/06/050Y
VC1	4pF-20pF, 250V, -10%+50%	03/07/0069
RESISTORS		
R1, R2	1kΩ, 250mW, 2%, 100ppm	01/01/0646
R3	2.2kΩ, 250mW, 2%, 100ppm	01/01/1642
R4, R5	1kΩ, 250mW, 2%, 100ppm	01/01/0646
R6, R7	2.2kΩ, 250mW, 2%, 100ppm	01/01/1642
R8	820Ω, 250mW, 2%, 100ppm	01/01/0611
R9	1kΩ, 250mW, 2%, 100ppm	01/01/0646
R10	8.2kΩ, 250mW, 2%, 100ppm	01/01/0921
R11	6.8kΩ, 250mW, 2%, 100ppm	01/01/0905
R12, R13	47kΩ, 250mW, 2%, 100ppm	01/01/1103
R14	8.2kΩ, 250mW, 2%, 100ppm	01/01/0921
R15	10kΩ, 250mW, 2%, 100ppm	
R16	4.7kΩ, 250mW, 2%, 100ppm	01/01/084Y
RESISTORS (Cont.)		
R17	33kΩ, 250mW, 2%, 100ppm	01/01/1065
R18	3.3kΩ, 250mW, 2%, 100ppm	01/01/0786
R19	82kΩ, 250mW, 2%, 100ppm	01/01/1154
R20	100kΩ, 250mW, 2%, 100ppm	01/01/1162
R21	15kΩ, 250mW, 2%, 100ppm	01/01/0972
R22	3.3kΩ, 250mW, 2%, 100ppm	01/01/0786
R23	82kΩ, 250mW, 2%, 100ppm	01/01/1154
R24	560Ω x 4, 125mW, 5%, 300ppm	01/08/1012
R25-R27	1kΩ, 250mW, 2%, 100ppm	01/01/0646
R28-R30	470Ω, 250mW, 2%, 100ppm	01/01/1103
VR1, VR2	5kΩ, 1W, 10%	02/01/0097
INTEGRATED CIRCUITS		
AA	74LS138N	04/01/109Y
AB	74LS174N	04/01/1422
AC, AD	10125P	04/01/2089
AE, AF	74S374N	04/01/4294
AG	74LS244N	04/01/2828
AH	74S240N	04/01/3786
BA	SPARE	
BB	10124P	04/01/207Y
BC, BD	10125P	04/01/2089
BF	74S374N	04/01/4294
BG	74LS14N	04/01/3425
BH	54-131	30/01/0264
CA	741CN	04/01/250X
CB	74LS125N	04/01/3603
CC, CD	85S68CP	04/01/5428
CG	74LS240N	04/01/2879
CH	74S374N	04/01/4294
DA	Crystal Osc. 14.318MHz	28/02/0236
DC	74S163N	04/01/370Y
DD	74S02N	04/01/0116
DE	74LS02N	04/01/1724
DF	74LS03PN	04/01/3085
DG	74S04N	04/01/0167
DH	Programmed set	
EA, EB	74LS221N	04/01/1589
ED-EF	74S163N	04/01/370Y
EG	Programmed set	
EH	74S174N	04/01/4219
FB	74LS221N	04/01/1589
FC	74LS74N	04/01/0728
FD-FF	74LS163N	04/01/1317
FG	Programmed set	
FH	74LS174N	04/01/1422
MISCELLANEOUS		
TR1	Transistor NPN ZTX107L	05/01/0268

17447 Component List



17447, Figure 1 Input Timing Card Block Diagram


TP2
C54
C12
W6
RN2
RN1
TP4
17447
AE
C13
C14
C15
C16
C17
C18
C19
AH
AG
AF
AD
AC
AB
AA
C55
C56
W6
R1
C20
C61
C21
C22
C23
C24
C25
C26
R25
BH
BG
BF
BD
BC
BB
BA NOT FITTED
R30
R2
W1
W2
W4
W3
R24
C57
C58
C59
C27
C28
C29
C30
C31
W1
W2
W3
W4
C1
C32
C2
R12
CH
CG
CD
CC
CB
R8
R9
R10
R11
CA
TP8
W5
LK4
A
B
LK3
C60
C33
C34
C35
C36
C37
C38
R26
R27
R14
D1
C39
R13
DH
DG
DF
DE
DD
DC
LK2
VC1
C6
R15
DA
R16
C5
C40
C41
C42
C43
C44
C45
C46
R3
R7
R17
R18
EH
EG
EF
EE
ED
R6
TR1
C8
EB
C7
R19
C62
EA
C63
C47
C48
C49
C50
C51
C52
R22
R21
C53
R20
R29
R28
FH
FG
FF
FE
FD
FC
C10
FB
C9
R4
R5
R23
LK1
VR1
VR2
TP1
TP5
TP6
TP7
TP3



	PAL	NTSC
PROM PROG.	17447B. DH	17447A. DH
	17447B. EG	17447.A EG
	17447B. FG	174 47A. FG
LINK 1	625	525
LINK 3	INSERT	INSERT
LINK 4	—•—	—॥—
DA	IQDVCX 03	IQDVCX 03
FREQUENCY	13.5 MHZ	14.318 MHZ
LINK 2a	LO	HI
b	LO	LO
c	HI	LO
d	HI	LO

Issue E 25.11.83

17447, Figure 2 Input Timing Card : Circuit Diagram and Component Layout

STORE ADDRESS CARD

17425

1. INTRODUCTION

This card controls the reading of the framestore at video rate and access to the store by the computer. With reference to the circuit diagram, the circuitry on the upper right consists of horizontal counters (HE, HF, HG) and vertical counters (FD, FC, FB) providing video read address. The horizontal chain is clocked at pixel rate (RPPCK). RHR provides a reset at the beginning of each line and loads an origin (RXSCROLL) from latches HD, GH. The vertical counters are clocked by RHR which is a double pulse, thus incrementing vertically by two lines. Even lines form field one, odd lines form field two. The vertical reset RVR overlaps both pulses at the start of field one but only one pulse at the start of field two giving one extra clock and selecting lines 1, 3, 5 etc.

2. CIRCUIT DESCRIPTION

Vertical and horizontal resets are modified by the PLT signal which is active if the palette or menu is to be displayed. The palette or menu uses lines 0 - 127 of the store and picture uses lines 128 onwards. Normally 128 is added by software to RVSCROLL (latched in GD, GC) but PLT forces a clear rather than a load so that reading starts at line 0. RHR, RVL and PLT signals are generated at the appropriate times by PROMs on the Output Timing card so that the menu appears at top or bottom as required.

Counters IF, IE allow for horizontal and vertical zoom by pixel replication. FLD SELECT can be used to force the vertical addresses to odd or even (V0 via IH) thus displaying only one field with lines replicated. These are used only for testing.

Horizontally the store is divided into ‘stripes’ of ten pixels. Each video read accesses a whole stripe and the pixels are demultiplexed by the output registers of the Store card. RA0 - RA3 are addresses within a stripe and are used as chip selects. H0 - H7 form addresses within the RAM array. OPRA and OPRB are the store output register (74LS670) read addresses, two used for video and two used for computer read data. OPRB selects between video and computer read on alternate pixels with AH (74S157) switching between video and computer stripe addresses.

The store cycle controls signals RAS, CAS etc., are generated by the block of circuitry shown at the bottom of the diagram. RREQ initiates a video read cycle every ten pixels. The request is latched in HB. It is released through HA when any current computer access cycle is cleared by LAAC, and is allowed through GB to clock EC when the current cycle ends as indicated by STORE BUSY. RAS, CAS, etc., are formed by the delay lines GF, GE and exclusive OR’s. MXR produces the RAS to CAS address change via the multiplexers DG, EG, FG, GG. These also switch between video read and computer access addresses with R/C select from IB. This will change on LAAC (Look Ahead Address Change) which is as soon as column addresses latched by CAS. The state of HC depends on whether the current cycle is video or computer access and routes LAAC via GB, HA to clear the current cycle. Selectors DF, EE perform address mapping to convert the store array from 640 x 1024 to 800 x 768.

Computer access is initiated by CREQ (A39) from the Brush Address card and acts in a similar way as RREQ. The gate EA (4, 5, 6) prevents a race between computer and video requests. Computer addresses come from counters CE, CF, CG (horizontal) and DB, DC, DD (vertical). These counters are controlled via the Address Control Bus AB12 to AB18 which is driven by the Brush Address during painting, the Size card for disc reads and Input Timing for live video write. CYLD, CYLD cause origins to be loaded from counters BE, BF, BG (horizontal) and DA, CB, CD (vertical). These can be loaded from the computer data bus and can be incremented or decremented as required for rotating cutouts. Computer origins CXPOS, CYPOS and video scrolls RVSCR, RXSCR are loaded from system bus when CSR = 2. With DC15 high both Store Address cards get loaded but with D15 low only Store II is loaded. STYPE (A29) is programmed on the backplane. D12 - D14 are decoded by BA to determine the destinations of Data D0 - D11. Horizontal positions and scrolls are divided by ten by PROMs BB, BC, BD to give stripe number (0 - 80) and address within stripe (0 - 9).

The store READ/WRITE signal (A27) is a copy of CR/W from the brush address, modified by PROTX and PROTY and latched for a cycle by HC. Store protect signals are generated by PROMs ED, DE which are controlled by inputs PROT A, B (A46, A45) which come from the Output Timing card. They are used for example to restrict drawing to the palette area.

IPSEL selects the input data buffer on the Store cards and is toggled by IPEN. The computer writes one pixel per computer access cycle except for live video (SVH high) when ten pixels are written per cycle. IPSEL then toggles every ten pixels. CCK (A20) is used to latch data at the output of the store on computer reads and CSEL selects between odd and even pixels in the store (CA0).

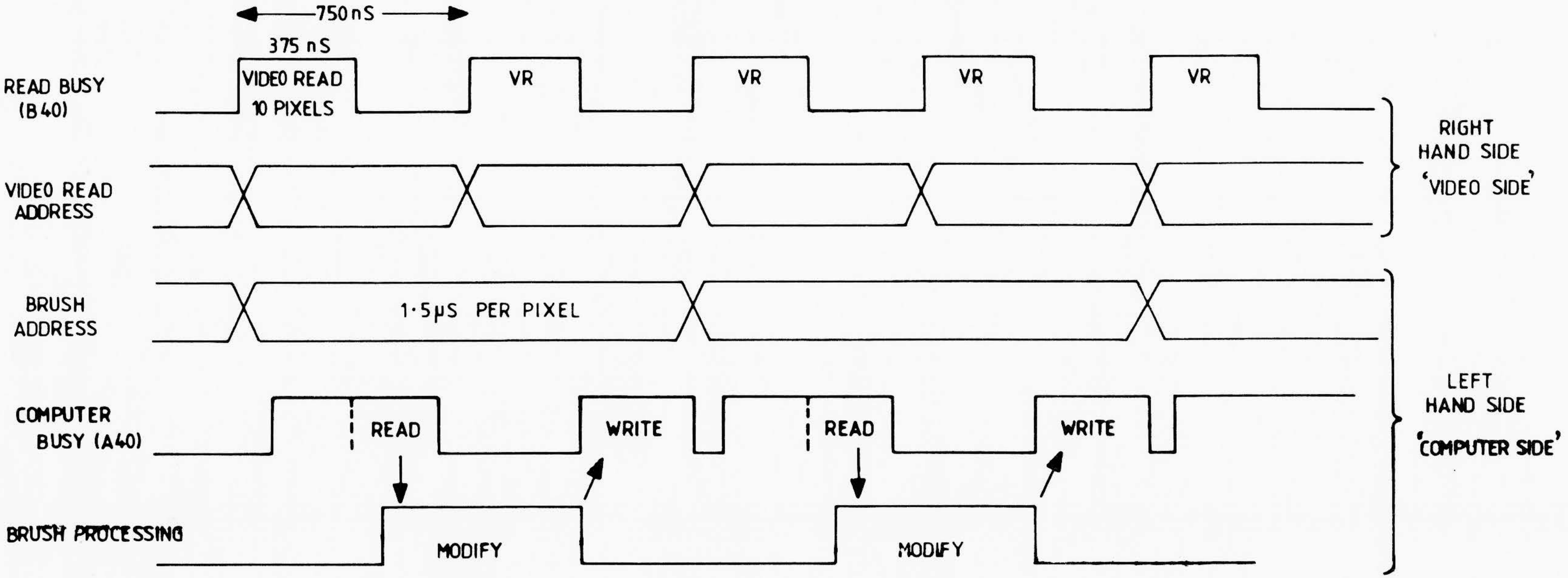
RBUSY and CBUSY inform the Brush Address when each store cycle ends.

Digital blanking of output video is provided by logic array IG. This is only active when a scroll is applied. The signal from each store address (BLK, B29) is fed to the combiner and used to select a matte colour. Blanking is disabled by the switch at the front of the card.

REF.	DESCRIPTION	STOCK CODE
CAPACITORS		
C1	180pF, 100V, 10%	03/06/039X
C2	120pF, 100V, 10%	03/01/0414
C3, C4	220pF, 100V, 10%	03/06/0055
C5	100pF, 100V, 10%	03/06/0306
C6	22µF, 16V, 20%	03/03/0253
C7-C77	100000pF, 50V, +80%-20%	03/06/0233
C78-C80	22µF, 16V, 20%	03/03/0253
RESISTORS		
R1	2.2kΩ, 250mW, 1%, 50ppm	01/01/0727
R2	1kΩ, 250mW, 2%, 100ppm	01/01/0646
R3, R4	2.2kΩ, 250mW, 1%, 50ppm	01/01/0727
R5	1kΩ, 250mW, 2%, 100ppm	01/01/0646
R6, R7	2.2kΩ, 250mW, 1%, 50ppm	01/01/0727
R8	270Ω, 250mW, 2%, 100ppm	01/01/0476
R9	200Ω, 250mW, 2%, 100ppm	01/01/0425
R10	2.2kΩ, 250mW, 1%, 50ppm	01/01/0727
R11	470Ω, 250mW, 2%, 100ppm	01/01/0557
R12, R13	220Ω, 250mW, 2%, 100ppm	01/01/0441
R14-R23	2.2kΩ, 250mW, 1%, 50ppm	01/01/0727
INTEGRATED CIRCUITS		
AA	74S260N	04/01/1597
AB-AD	74LS244N	04/01/2828
AE	74LS240N	04/01/2879
AF	74S00N	04/01/0035
AG	74LS244N	04/01/2828
AH	74S157N	04/01/121X
BA	74LS138N	04/01/109Y
BB-BD	Programmed set make from Ref. only S x 04/01/5339 93455 1 x 04/01/6874 16L2	
BE	74LS168A	04/01/8559
BF, BG	74LS169A	04/01/6734
BH	74S74N	04/01/0698

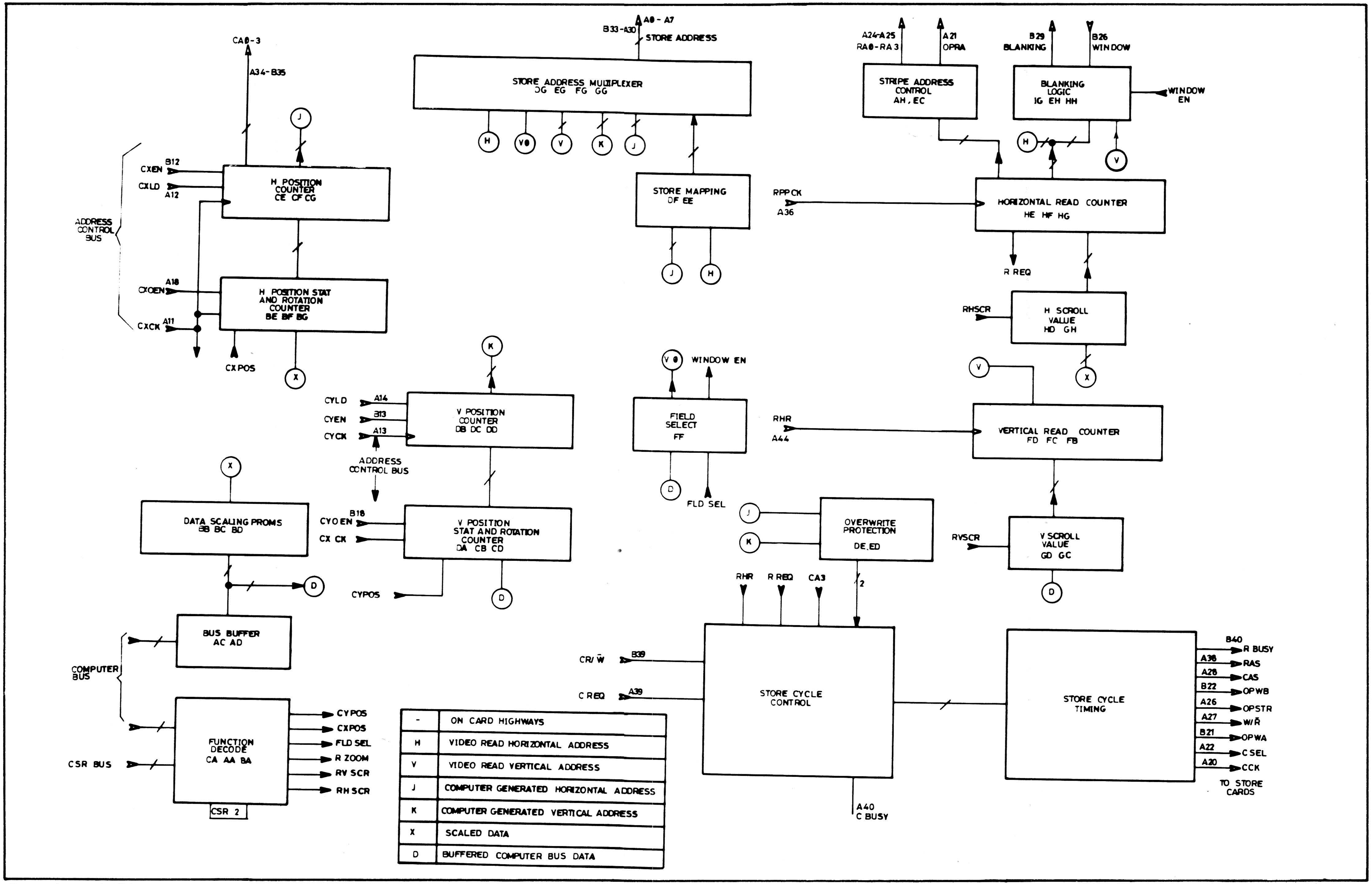
REF.	DESCRIPTION	STOCK CODE
INTEGRATED CIRCUITS (Cont.)		
CA	74LS14N	04/01/3425
CB	74LS169A	04/01/0698
CC	74S174N	04/01/4219
CD	74LS169A	04/01/0698
CE	74S168N	04/01/6033
CF, CG	74S169N	04/01/1368
CH	74LS86N	04/01/0833
DA-DD	74LS169A	04/01/0698
DE	Programmed set make from Ref. only S x 04/01/5339 93455 1 x 04/01/6874 16L2	
DF	74S157N	04/01/121X
DG	74LS153N	04/01/118X
DH	74S02N	04/01/0116
EA	74S00N	04/01/0035
EB	74S04N	04/01/0167
EC	74S74N	04/01/0698
ED	Programmed set make from Ref. only S x 04/01/5339 93455 1 x 04/01/6874 16L2	
EE	74S157N	04/01/121X
EF	74S86N	04/01/0825
EG	74LS153N	04/01/118X
EH	74S74N	04/01/0698
FA	74S00N	04/01/0035
FB-FD	74LS163N	04/01/1317
FE	74S86N	04/01/0825
FF	74LS175N	04/01/1457
FG	74LS153N	04/01/118X
FH	74S32N	04/01/0485
GA	74S02N	04/01/0116
GB	74LS00N	04/01/006X
GC, GD	74LS174N	04/01/1422
GE, GF	54-134	30/01/028Y
GG	74LS153N	04/01/118X
GH	74LS174N	04/01/1422
HA	74S08N	04/01/0256
HB, HC	74S74N	04/01/0698
HD	74LS174N	04/01/1422
HE	74S162N	04/01/6866
HF, HG	74S163N	04/01/370Y
HH	74LS164N	04/01/3719
IA, IB	74S74N	04/01/0698
IC	74S00N	04/01/0035
ID	74LS175N	04/01/1457
IE	74LS163N	04/01/1317
IF	74S163N	04/01/370Y
IG	Programmed set make from Ref. only S x 04/01/5339 93455 1 x 04/01/6874 16L2	
IH	74LS00N	04/01/006X

17425 Component List



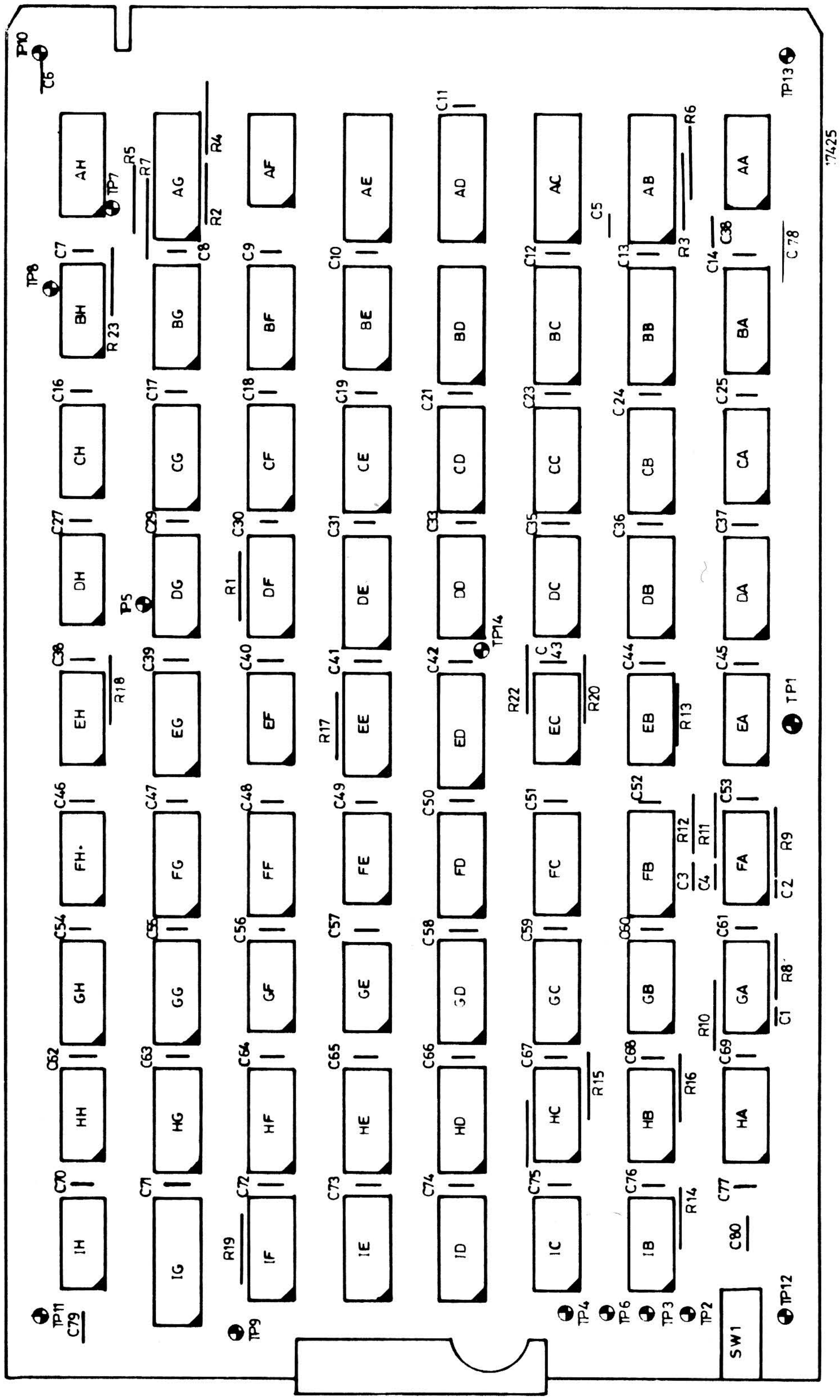
TRANSFER	ADDRESS CONTROL BUS MASTER	PIXEL-TIME
PAINTING	BRUSH ADDRESS	1·5μs
FAST WIPE	BRUSH ADDRESS	750n sec
DISC	SIZE CARD	2·0μs
LIVE VIDEO	INPUT TIMING	75n sec
DIGITAL LINK	BRUSH ADDRESS	3·6μs

17425, Figure 1 Store Address Card Timing Diagrams



-	ON CARD HIGHWAYS
H	VIDEO READ HORIZONTAL ADDRESS
V	VIDEO READ VERTICAL ADDRESS
J	COMPUTER GENERATED HORIZONTAL ADDRESS
K	COMPUTER GENERATED VERTICAL ADDRESS
X	SCALED DATA
D	BUFFERED COMPUTER BUS DATA

17425, Figure 2 Store Address Card Block Diagram


AA
AB
AC
AD
AE
AF
AG
AH
BA
BB
BC
BD
BE
BF
BG
BH
CA
CB
CC
CD
CE
CF
CG
CH
DA
DB
DC
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IE
IF
IG
IH
TP1
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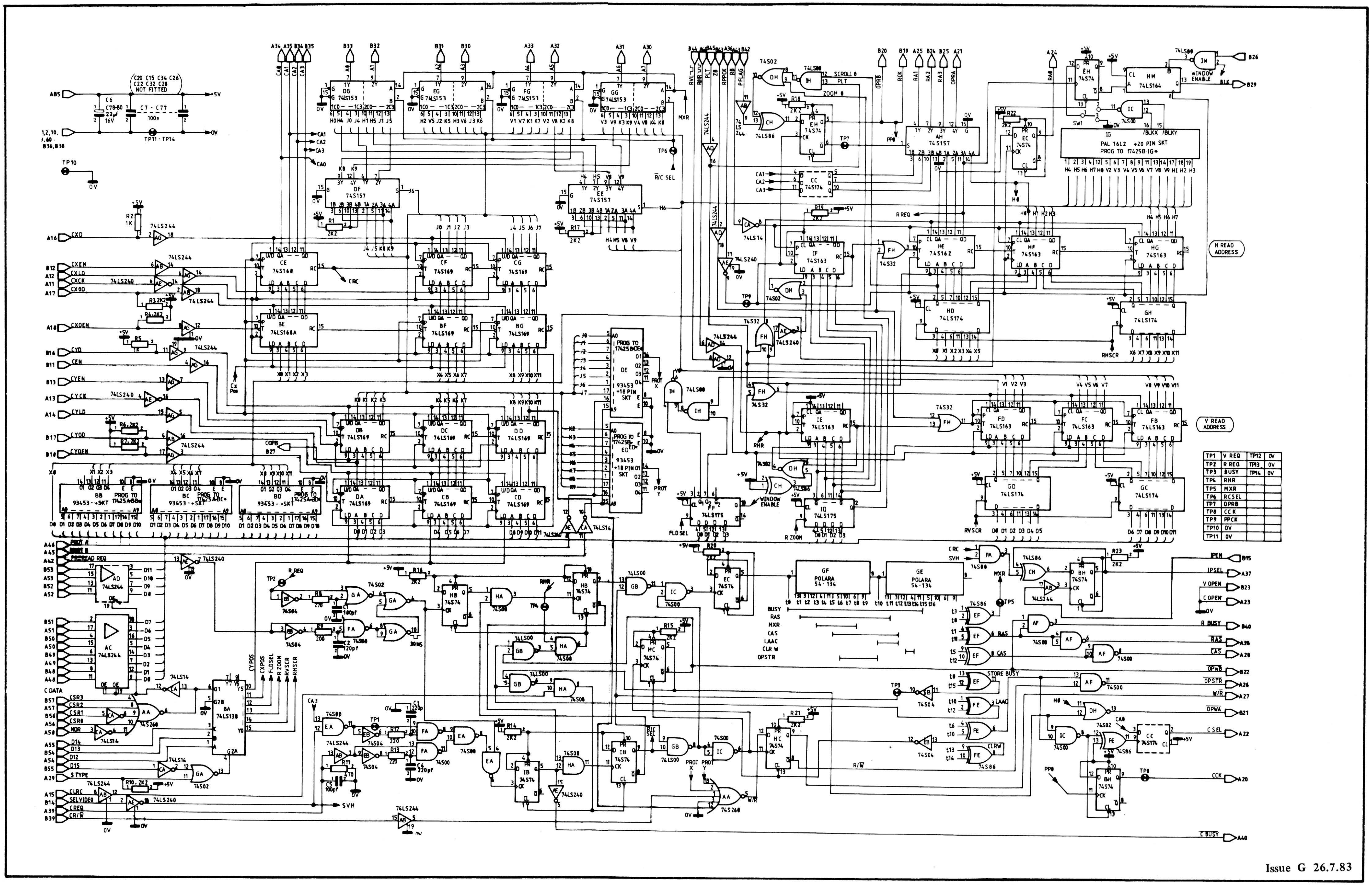
TP13
TP14
SW1
17425



TP1	V REQ	TP12	0V
TP2	R REQ	TP13	0V
TP3	BUSY	TP14	0V
TP4	RHR		
TP5	MXR		
TP6	RCSEL		
TP7	OPRB		
TP8	CCK		
TP9	PPCK		
TP10	0V		
TP11	0V		

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17425, Figure 3 Store Address Card : Circuit Diagram and Component Layout

FRAMESTORE CARD

17420

1. INTRODUCTION

The system contains six identical Framestore cards. Each card provides storage for 8-bits of picture information. The system further splits the framestore into two groups of three cards with a separate Store Address controlling each group.

2. CIRCUIT DESCRIPTION

The storage within the Framestore card is divided into ten stripes each consisting of eight 64k RAMs and four 74LS670 multiplexing latches. All the RAMs are cycled together and will therefore require 10 x 8-bits of data simultaneously during a write cycle.

The 74LS670 is a 4 x 4-bit register array. It is used to collect the input data stream until there is sufficient data for a write cycle. It then presents this data to RAMs whilst continuing to collect the new input data stream into its second register. The first set of data will have been written to the RAMs before the second set of data is completely collected and so the first register will be available in time to collect the third set of input data. This flipping of registers between data input and data output continues indefinitely under the control of IPSEL (Input Select), which drives the 74LS670 Read Address (RA) and is used invert to drive the Write Address (WA).

The input data stream is presented to all the 74LS670 inputs, which are then sequentially write enabled by signals IPENO to IPEN9. These are decoded by two 74LS138s BA, CA from the low bits of the store address WA), WA1, WA2, WA3, a board select BDSEL and the overall timing signal IPEN. The low bits of the store address are designed to count in modulo 10 form so sequencing all the 74LS670s correctly.

Two modes of writing to the RAMs are available depending on the signal WHP. With this signal asserted, all the RAM stripes are written to, otherwise only one stripe is written to. This is determined by the PALs AB, BB. If WHP is asserted, or R/W indicates read mode, and the card is enabled by LUMEN, then RAS is passed onto all the RAMs. However, if WHP is not asserted, the low bits of the store address WA0, WA1, WA2 and WA3 are latched within the PALs by IPEN and used to determine which stripe of RAMs should be allowed the next RAS pulse. One and only one stripe will be given an RAS pulse in this mode of operation.

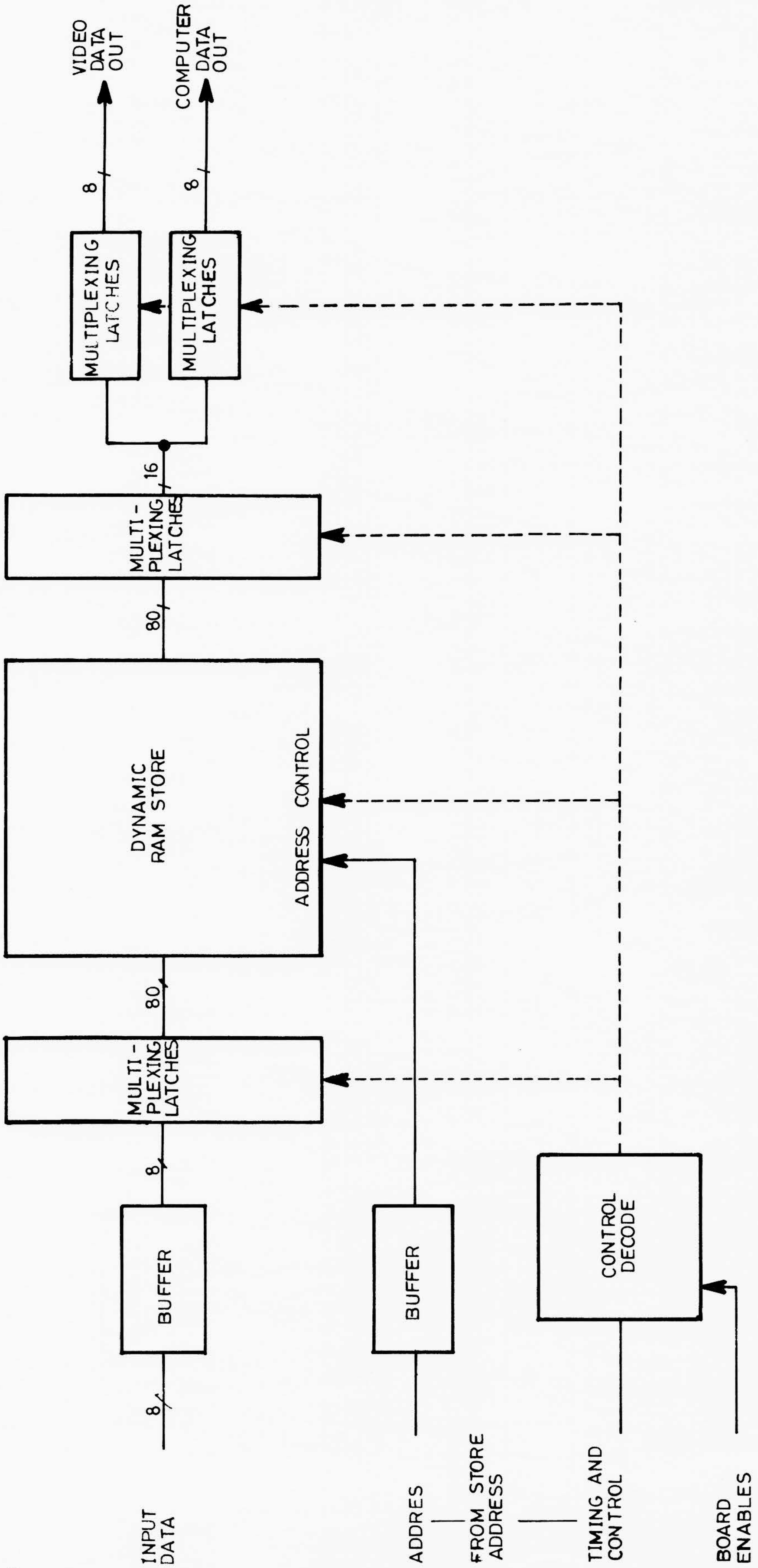
During a RAM cycle the store address provides the multiplexer address, RAS, CAS and an R/W select. These are buffered by chips CB, CC, CD, CE, BC and AD before being sent on to the RAM chips.

The output 74LS670s operate in a similar manner to the input except that a computer read cycle may be inserted between each video read cycle. The double buffering for video access uses registers 0 and 1 while registers 2 and 3 are used for the computer access. Thus OPWB and OPRB determine whether the access is to video or computer data, and OPWA and OPRA determine the polarity of the enable buffering. These signals which are generated by the store address are buffered by AD before being passed to the 74LS670s. OPSTR is used to strobe the data into the 74LS670s at the end of a RAM read cycle. A 74LS138 is used to decode the low bits of the read store address RA1, RA2, RA3 to generate OPEN1 to OPEN5 sequentially output enabling each 74LS670 in turn. Since both video and computer data need to be fetched from the card' the multiplexing is done in two stages. The 74LS670s provide 8-bit to 16-bit multiplexing while the 74LS374s AF, BF, AE, BE provide 16-bit to 8-bit multiplexing for video and computer data respectively. This allows video and computer data to be sent alternately along the 16-bit internal hi-way, so allowing apparently simultaneous access. A 74LS139 BD decodes the lowest bit of the read store address RA0, output enabling AF or BF, and AE or BE, so completing the final stage of multiplexing. Data is clocked into these 74LS374 latches are the correct time by signals RCK and CCK which are generated by the store address.

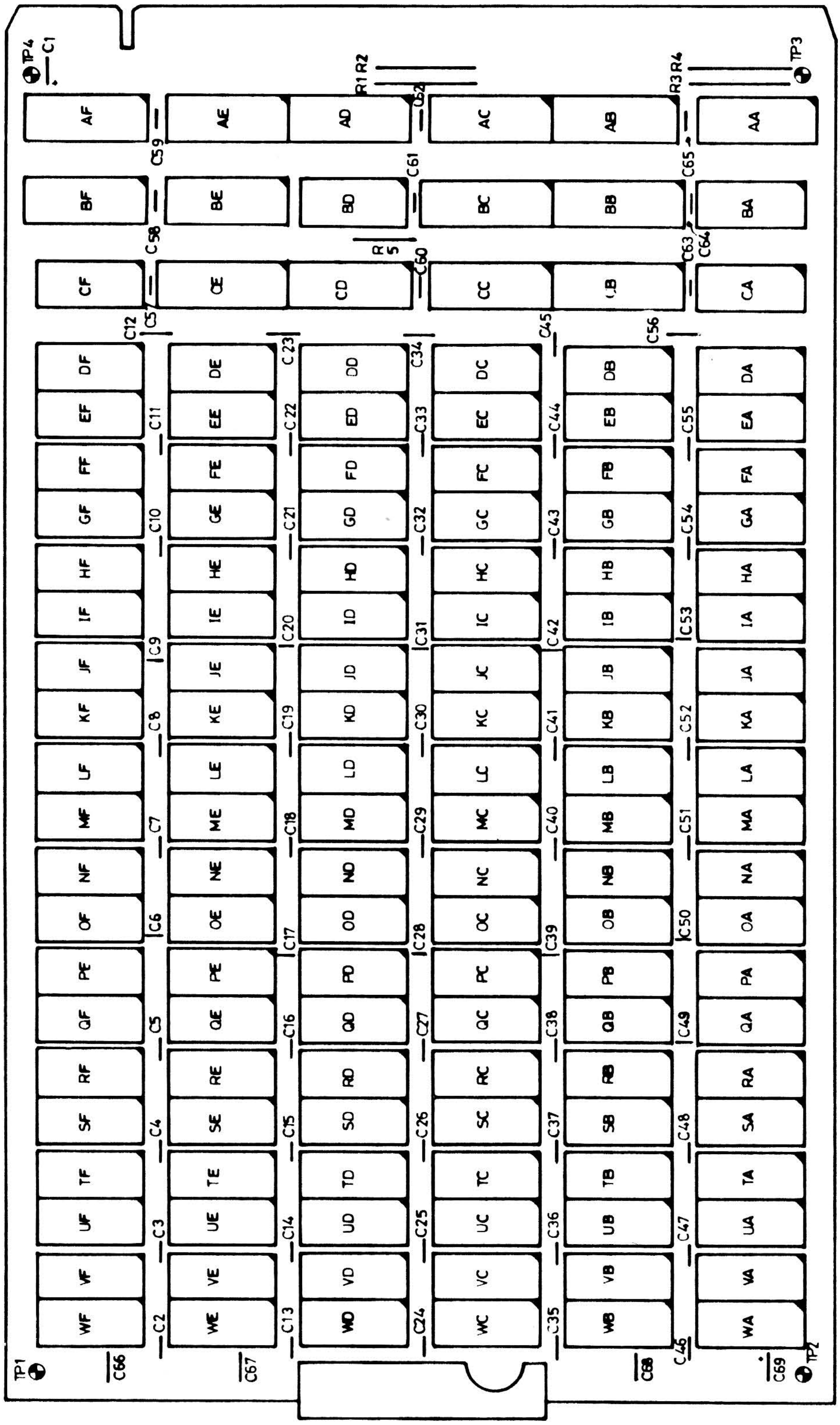
REF.	DESCRIPTION	STOCK CODE
CAPACITORS		
C1	22μF, 16V, 20%	03/03/0253
C2-C5	100000pF, 50V, +80%-20%	03/06/0233
C6	22μF, 16V, 20%	03/03/0253
C7, C8	100000pF, 50V, +80%-20%	03/06/0233
C9	22μF, 16V, 20%	03/03/0253
C10, C11	100000pF, 50V, +80%-20%	03/06/0233
C12	22μF, 16V, 20%	03/03/0253
C13-C16	100000pF, 50V, +80%-20%	03/06/0233
C17	22μF, 16V, 20%	03/03/0253
C18, C19	100000pF, 50V, +80%-20%	03/06/0233
C20	22μF, 16V, 20%	03/03/0253
C21, C22	100000pF, 50V, +80%-20%	03/06/0233
C23	22μF, 16V, 20%	03/03/0253
C24-C27	100000pF, 50V, +80%-20%	03/06/0233
C28	22μF, 16V, 20%	03/03/0253
C29, C30	100000pF, 50V, +80%-20%	03/06/0233
C31	22μF, 16V, 20%	03/03/0253
C32, C33	100000pF, 50V, +80%-20%	03/06/0233
C34	22μF, 16V, 20%	03/03/0253
C35-C38	100000pF, 50V, +80%-20%	03/06/0233
C39	22μF, 16V, 20%	03/03/0253
C40, C41	100000pF, 50V, +80%-20%	03/06/0233
C42	22μF, 16V, 20%	03/03/0253
C43-C48	100000pF, 50V, +80%-20%	03/06/0233
C49, C50	22μF, 16V, 20%	03/03/0253
C51, C52	100000pF, 50V, +80%-20%	03/06/0233
C53	22μF, 16V, 20%	03/03/0253
C54, C55	100000pF, 50V, +80%-20%	03/06/0233
C56	22μF, 16V, 20%	03/03/0253
C57-C65	100000pF, 50V, +80%-20%	03/06/0233
RESISTORS		
R1-R4	NOT FITTED	
R5	2.2kΩ, 250mW, 2%, 100ppm	01/01/1642

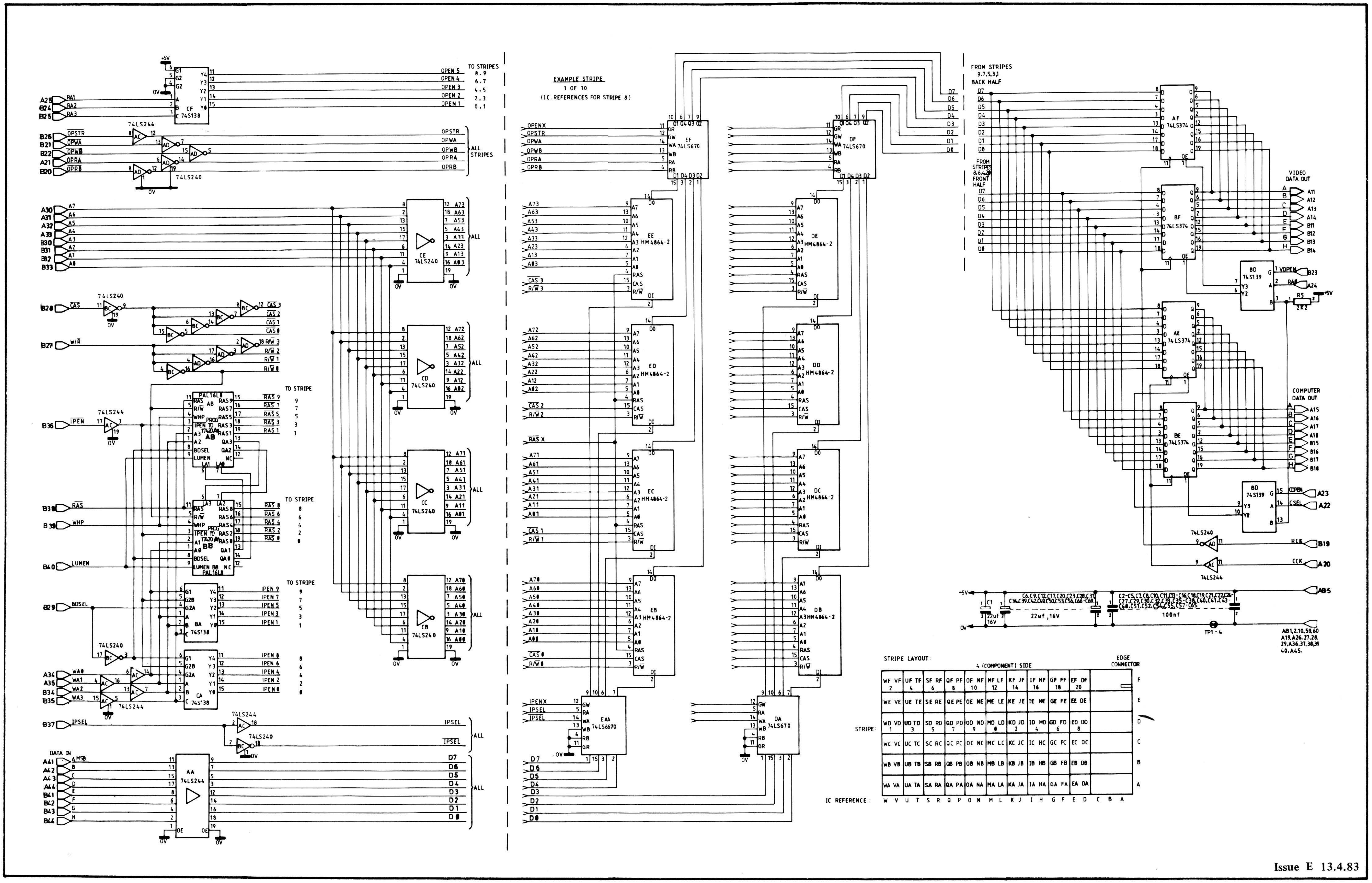
REF.	DESCRIPTION	STOCK CODE
INTEGRATED CIRCUITS		
AA, AC	74LS244N	04/01/2828
AD	74LS240N	
AE, AF	74LS374P	04/01/8427
BA	74S138N	04/01/1082
BC	74LS240N	
BD	74S139N	04/01/420Y
BE	74LS374P	04/01/1082
BF	TEXAS OR FAIRCHILD	
CA	74S138N	04/01/1082
CB-CD	74LS240N	04/01/2879
CF	74S138N	04/01/1082
DA	74LS670N	04/01/4332
DB-DE	4864-2	
DF, EA	74LS670N	04/01/4332
EB-EE	4864-2	
EF, GA	74LS138N	04/01/1082
GB-GE	4864-2	
GF, HA	74LS670N	04/01/4332
HB-HE	4864-2	
HF, IA	74LS670N	04/01/4332
IB-IE	4864-2	
IF, JA	74LS670N	04/01/4332
JB-JE	4864-2	
JF, KA	74LS670N	04/01/4332
KB-KE	4864-2	
KF, LA	74LS670N	04/01/4332
LB-LE	4864-2	
LF, MA	74LS670N	04/01/4332
MB-ME	4864-2	
MF, NA	74LS670N	04/01/4332
NB-NE	4864-2	
NF, OA	74LS670N	04/01/4332
OB-OE	4864-2	
OF, PA	74LS670N	04/01/4332
PB-PE	4864-2	
PF, QA	74LS670N	04/01/4332
QB-QE	4864-2	
QF, RA	74LS670N	04/01/4332
RB-RE	4864-2	
RF, SA	74LS670N	04/01/4332
SB-SE	4864-2	
SF, TA	74LS670N	04/01/4332
TB-TE	4864-2	
TF, UA	74LS670N	04/01/4332
UB-UE	4864-2	
UF, VA	74LS670N	04/01/4332
VB-VE	4864-2	
VF, WA	74LS670N	04/01/4332
WB-WE	4864-2	
WF	74LS670N	04/01/4332

17420 Component List



17420, Figure 1 Framestore Card Block Diagram


TP4
C1
TP3
R1 R2
R3 R4
R5
AF AE AD AC AB AA
BF BE BD BC BB BA
CF CE CD CC CB CA
DF DE DD DC DB DA
EF EE ED EC EB EA
FF FE FD FC FB FA
GF GE GD GC GB GA
HF HE HD HC HB HA
IF IE ID IC IB IA
JF JE JD JC JB JA
KF KE KD KC KB KA
LF LE LD LC LB LA
MF ME MD MC MB MA
NF NE ND NC NB NA
OF OE OD OC OB OA
PF PE PD PC PB PA
QF QE QD QC QB QA
RF RE RD RC RB RA
SF SE SD SC SB SA
TF TE TD TC TB TA
UF UE UD UC UB UA
VF VE VD VC VB VA
WF WE WD WC WB WA
C2 C3 C4 C5 C6 C7 C8 C9 C10 C11 C12
C13 C14 C15 C16 C17 C18 C19 C20 C21 C22 C23
C24 C25 C26 C27 C28 C29 C30 C31 C32 C33 C34
C35 C36 C37 C38 C39 C40 C41 C42 C43 C44 C45
C46 C47 C48 C49 C50 C51 C52 C53 C54 C55 C56
C57 C58 C59 C60 C61 C62 C63 C64 C65
C66 C67 C68 C69
TP1
TP2
17420


TO STRIPES
CF 74LS138
OPEN 5
OPEN 4
OPEN 3
OPEN 2
OPEN 1
OPSTR
OPWA
OPWB
OPRA
OPRB
ALL STRIPES
74LS244
74LS240
CE 74LS240
CD 74LS240
CC 74LS240
CB 74LS240
PAL16L8 AB
PAL16L8 BB
BA 74S138
CA 74S138
AA 74LS244
DATA IN
EXAMPLE STRIPE
1 OF 10
(I.C. REFERENCES FOR STRIPE 8)
EF 74LS670
DF 74LS670
EE HM4864-2
DE HM4864-2
ED HM4864-2
DD HM4864-2
EC HM4864-2
DC HM4864-2
EB HM4864-2
DB HM4864-2
EA 74LS670
DA 74LS670
FROM STRIPES 9,7,5,3,1 BACK HALF
FROM STRIPES 8,6,4,2,0 FRONT HALF
AF 74LS374
BF 74LS374
AE 74LS374
BE 74LS374
BD 74S139
VIDEO DATA OUT
COMPUTER DATA OUT
RCK
CCK
22uf 16V
22uf ,16V
100nf
TP1 - 4
STRIPE LAYOUT:
4 (COMPONENT) SIDE
EDGE CONNECTOR
STRIPE:
WF VF 2 | UF TF 4 | SF RF 6 | QF PF 8 | OF NF 10 | MF LF 12 | KF JF 14 | IF HF 16 | GF FF 18 | EF DF 20 | F
WE VE | UE TE | SE RE | QE PE | OE NE | ME LE | KE JE | IE HE | GE FE | EE DE | E
WD VD 1 | UD TD 3 | SD RD 5 | QD PD 7 | OD ND 9 | MD LD 0 | KD JD 2 | ID HD 4 | GD FD 6 | ED DD 8 | D
WC VC | UC TC | SC RC | QC PC | OC NC | MC LC | KC JC | IC HC | GC FC | EC DC | C
WB VB | UB TB | SB RB | QB PB | OB NB | MB LB | KB JB | IB HB | GB FB | EB DB | B
WA VA | UA TA | SA RA | QA PA | OA NA | MA LA | KA JA | IA HA | GA FA | EA DA | A
IC REFERENCE: W V U T S R Q P O N M L K J I H G F E D C B A

Issue E 13.4.83

17420, Figure 2 Framestore Card: Circuit Diagram and Component Layout

COMBINER CARD

17424

1. INTRODUCTION

This card takes the signals from the six framestores and combines them together in a programmable manner to produce a single full colour output.

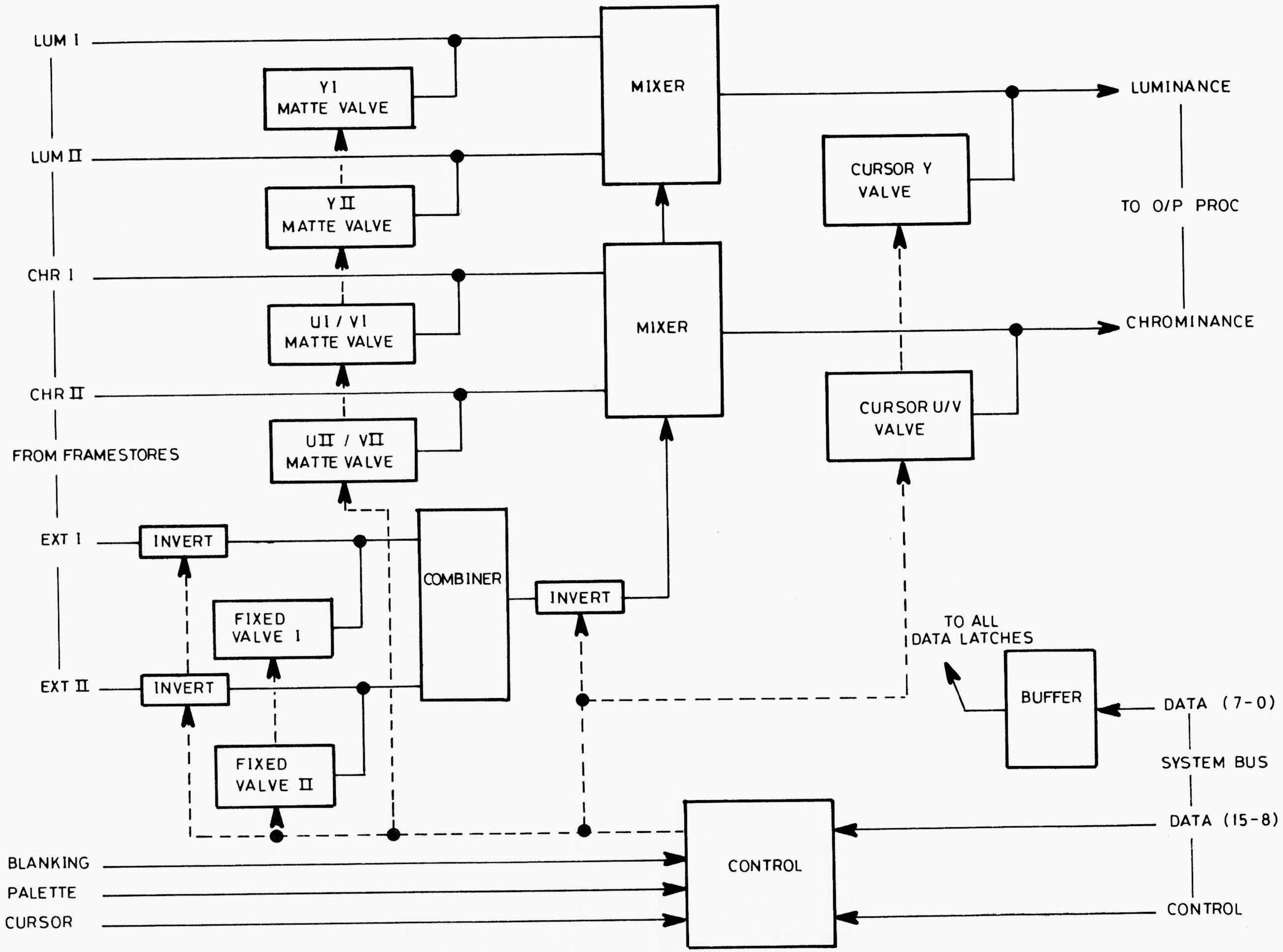
2. CIRCUIT DESCRIPTION

The two extension stores are conditionally inverted using PALs BA and BB before being combined together by multiplier GA. The output from this multiplier is made available in both normal and complemented form using the Ex-OR gates FC, FE, EE and EF. These are fed to two separate combiner paths, the luminance path and the chrominance path. Luminance from Store 1 is latched by AH whose output is tri-stated with an optional matte value which is loaded into the latch BH. The control signal to select matte or store data is held in the latch DH. The signal is then latched again by CH to compensate for delays along the extension route before being fed to the multiplier GE. Similary, luminance 2 follows a path through 74LS374s AG and CG before being presented to the multiplier GD. These two multipliers are fed with complementary values from the extension stores and their outputs added together, to form a mixing circuit where the value coming from the extension store multiplier determines the proportion in which these two stores are mixed. A similar circuit exists for the chrominance path exception that the matte value registers are duplicated so as to provide a R-Y and a B-Y component. Matte value from latches CB, CA may be selected instead of the data from the extension stores. Blanking signals from the Store Address cards (BLKI, BLKII) force the combiner to output matte values when the store is scrolled outside picture area. PLTL (B47) forces the combiner to display a menu, which menu is seen being determined by Q4 of FF.

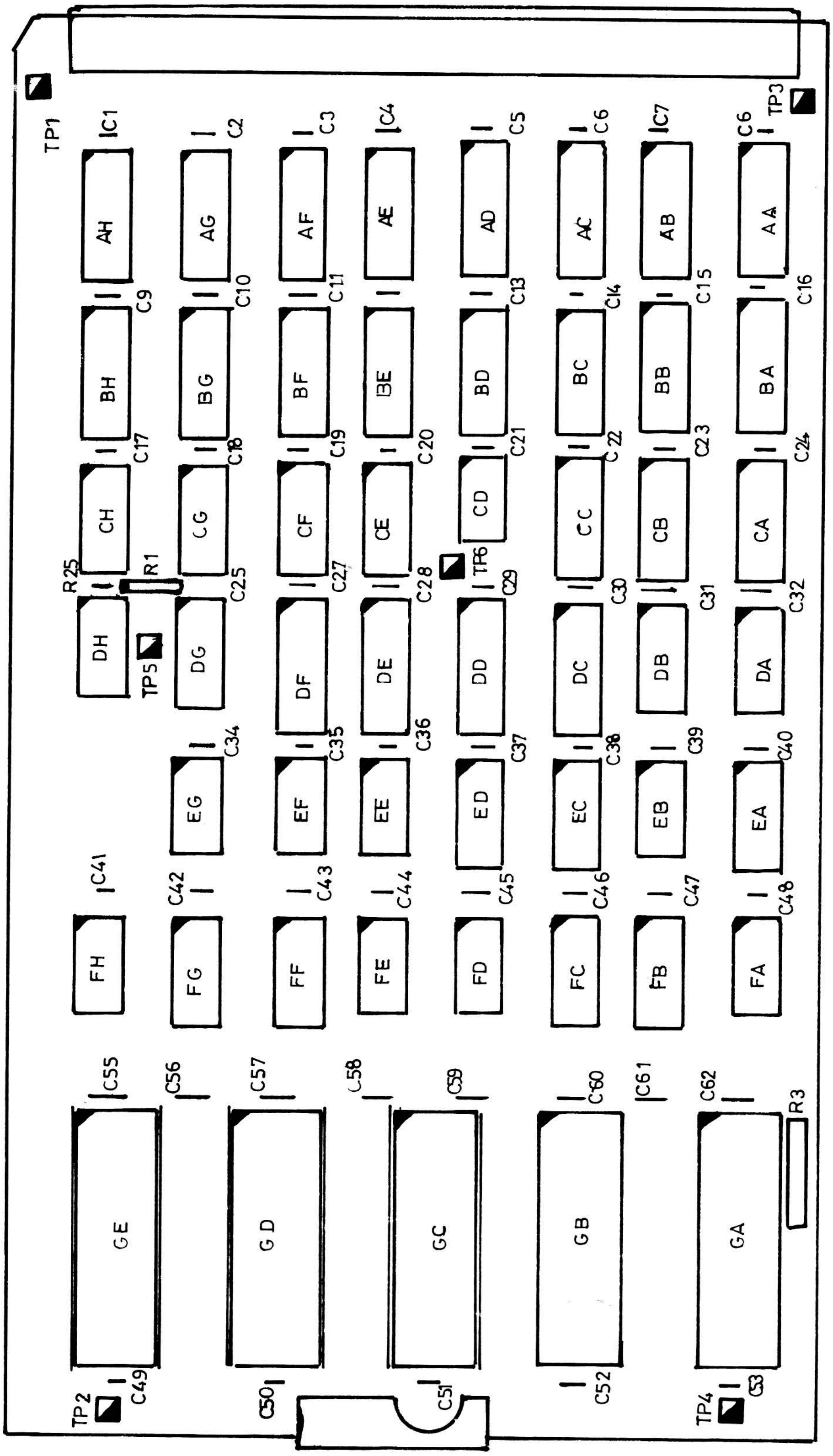
After the luminance stores are added together in adders ED and FC, they are latched once more in the 74LS374 DD. This is fed out onto the hi-way to the output processor but is also tri-stated with the cursor colour latch DD and drop shadow generator AD. The control signal for this tri-stating comes from the output timing and allows the cursor to be added to the VIDEO OUTPUT signal. Once again the colour latches are duplicated from the chrominance path (EC, CC) to allow both R-Y and B-Y components to be stored. Control signals on MS data bits from the system bus are decoded by three 74LS138s (DA, DB, EA), generating the latching clocks for sixteen possible destinations for the 8-bit data being passed onto the card via buffer AA.

REF.	DESCRIPTION	STOCK CODE
CAPACITORS		
C1-C32	10000pF, 100V, +80%-20%	06/03/0101
C33	NOT FITTED	
C34-C53	1000pF, 100V, +80%-20%	
C54-C62	22µF, 16V, 20%	03/03/0253
RESISTORS		
R1	1kΩ, 250mW, 1%, 50ppm	01/01/0638
R2	NOT FITTED	
R3	1kΩ x 8, 125mW, 5%, 300ppm	01/08/0539
INTEGRATED CIRCUITS		
AA	74LS244N	04/01/2828
AB	74LS240N	04/01/2879
AC, AD	74S240N	04/01/3786
AE-AH	74LS374N	04/01/3328
BC, BD	74S374N	04/01/4294
BE-CB	74LS374N	04/01/3328
CC	74S374N	04/01/4294
CD	74S74N	04/01/0698
CE-CH	74LS374N	04/01/3328
DA, DB	74LS138N	
DC, DD	74S374N	04/01/4294
DE, DF	74LS374N	04/01/3328
DG	74S175N	04/01/1449
DH	74LS74N	04/01/0728
EA	74LS138N	
EB	74S00N	04/01/0035
EC, ED	74S283N	04/01/4286
EE, EF	74S86N	04/01/0825
EG	74S00N	04/01/0035
EH	NOT FITTED	
FA	74S132N	04/01/4944
FB, FC	74S283N	04/01/4286
FD, FE	74S86N	04/01/0825
FF	74LS175N	04/01/1457
FG	74S157N	04/01/121X
FH	74S32N	04/01/0485
GA-GE	8HUJ-1	04/01/5908

17424 Component List



17424, Figure 1 Combiner Card Block Diagram


TP1
TP3
C1
C2
C3
C4
C5
C6
C7
C6
AH
AG
AF
AE
AD
AC
AB
AA
C9
C10
C11
C13
C14
C15
C16
BH
BG
BF
BE
BD
BC
BB
BA
C17
C18
C19
C20
C21
C22
C23
C24
CH
CG
CF
CE
CD
CC
CB
CA
R25
R1
TP6
C25
C27
C28
C29
C30
C31
C32
DH
TP5
DG
DF
DE
DD
DC
DB
DA
C34
C35
C36
C37
C38
C39
C40
EG
EF
EE
ED
EC
EB
EA
C41
C42
C43
C44
C45
C46
C47
C48
FH
FG
FF
FE
FD
FC
FB
FA
C55
C56
C57
C58
C59
C60
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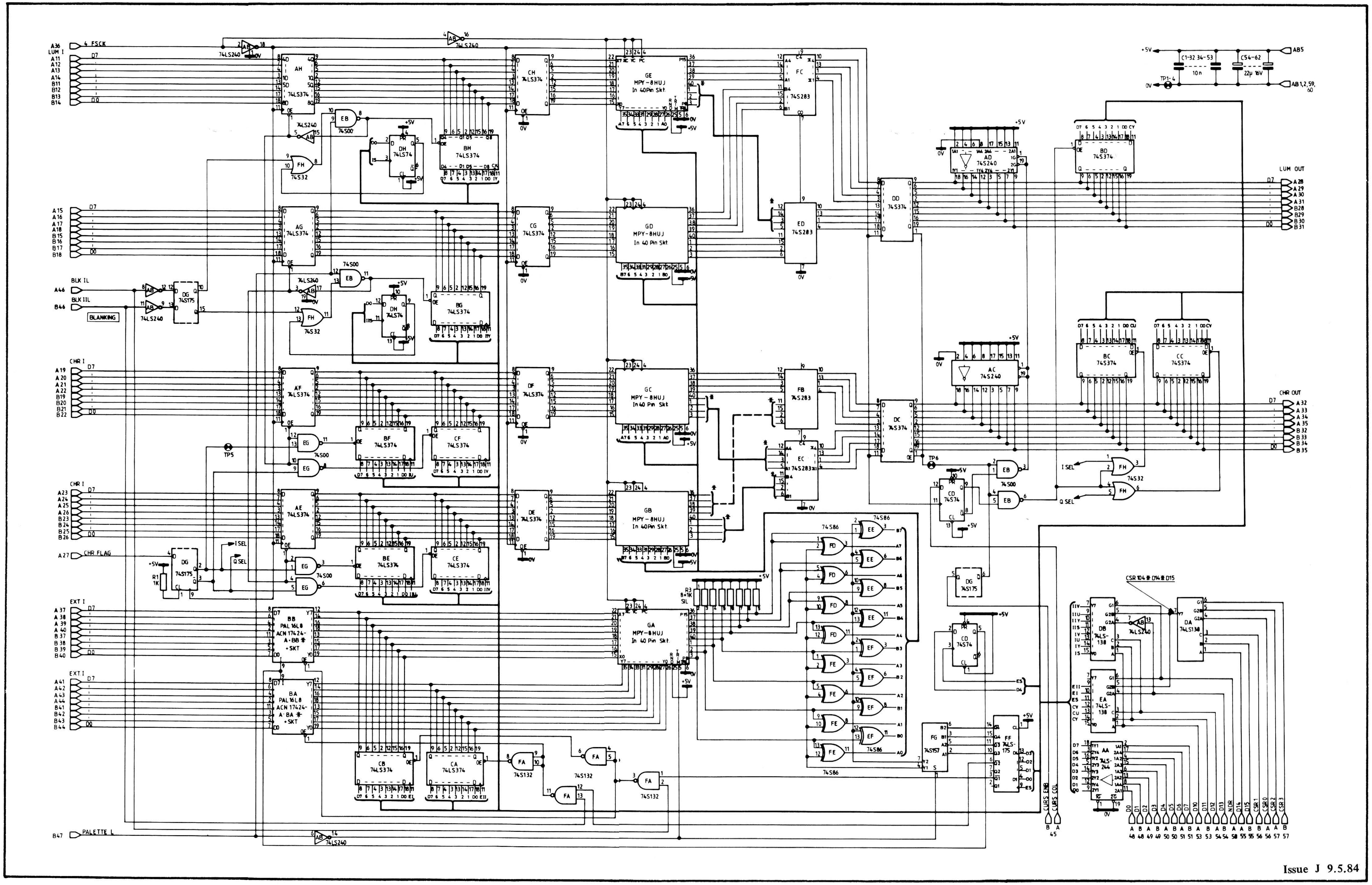
C62
R3
GE
GD
GC
GB
GA
TP2
C49
C50
C51
C52
TP4
C53



17424, Figure 2 Combiner Card : Circuit Diagram and Component Layout

OUTPUT TIMING CARD

17418

1. INTRODUCTION

The Output Timing card serves three functions:

(a) To generate all the timing signals for the system and make sure that they are gen-locked to the incoming locking signal.

(b) To store the cursor parameters and generate the timing signals required to place the cursor colours onto the video output.

(c) To provide 32 switches readable by the system computer to act as configuration switches for the software.

2. CIRCUIT DESCRIPTION

Horizontal and vertical syncs are provided as TTL signals from the Output Locking card. When the horizontal counters AH, BH and CH form a final ripple carry, they re-load themselves to the complement of the number of clocks per line. This in turn triggers the H0 monostable FE whose output provides the reference edge for the phase comparator. The horizontal counters are designed to re-load themselves before the next horizontal sync position so allowing the H0 monostable to be varied both positive and negative of the reference syncs. Latches DH and gates EH form a phase comparator, comparing the H0 monostable output to the H sync input. It provides pump-up and pump-down information for the capacitor C59. The resultant voltage is integrated by op-amp FH and fed to the variable capacitance diode D2 so controlling the oscillator (FG) frequency and thus phase locking the counters. The vertical counters CG, DG and EG are crash locked by the vertical syncs via monostable FE and latch GE. In the event of there being no GEN-LOCK signal, both horizontal and vertical counters are designed to free-run providing the system with its necessary clocks so that it may continue to operate.

The horizontal counter is divided up into sixteen states each of an appropriate length using the PROM BG. Similarly, the vertical half line counter also splits up into vertical states using the PROM BF. After being latched these states are fed into the combiner PROMs BF and BE so producing the final output signals from the matrix of horizontal and vertical states. PROM BE also takes in two control signals. These are PALETTE ON and PALETTE TOP or BOTTOM. The output signals from this PROM are then dependent upon whether and where the palette is positioned.

The cursor is defined by four parameters:

(a) Horizontal Origin.

(b) Vertical Origin.

(c) Horizontal Length.

(d) Vertical Length.

These are all stored in the 4 x 12 register formed by the 74LS670s BA, CB and CC. The data on the output of these depend upon the horizontal and vertical timing signals. During read horizontal reset, the vertical information is output whilst the horizontal data is output during the rest of the line. Horizontal origin is output during the pre-request part of the line and the horizontal counters loaded at this stage. When allowed to run by cursor enable these counters (DC, DB and DA) count up until they carry over. They re-load themselves with the horizontal length which is now selected on the data hi-way. At the same time, the cursor address counters FC, FB are cleared to zero. These are allowed to count up to the value of fifteen while the horizontal length is also being counted. When they reach fifteen, they hold until allowed to continue by the horizontal length counter carry over. When the counters FC and FB reach 31, the whole system is disabled until re-started on the next line. Counters FC and FB operate in two stages so that the box cursor may be of any size.

The vertical counters EC, EB and DA and vertical cursor address counter FD and FC operate in a similar manner but during the timing pulses of RHR and RVR. The 5-bit horizontal address and 5-bit vertical address are fed into PROM CD which has been programmed with the cursor shapes. Outputs 1 and 2 give the cursor cross-shape defining both signal and drop shadow while outputs 3 and 4 provide signal and drop shadow for the box cursor. This signal selector is latched from the system first in latches AC. A filled rectangular box is also available at the cursor, which is generated by using just the MS bit of the horizontal and vertical addresses gated by AND gate AB. This is made available through the cursor path selector AD. If the cursor type is zero then no cursor will be displayed.

The final function of this card is to allow switches 1 - 4 to be read by the computer. They are read as two 16-bit words (CSR codes 12 and 14) which are enabled on to the system hi-way using the 74LS244s HC, GC, HA and GA. Switch OFF places a high on the bus, while switch ON places a low on the bus. Software normally complements this data before use.

SOFTWARE V2.0 ADDITIONS TO CONFIGURATION SWITCHES

(a) Honeywell 3000 Camera.

Setting switch HD8 on = camera present. Expose box will appear on full page memory, together with film type selection.

Pressing the expose box will trigger the camera.

(b) Cue Dot

Setting switch HD4 on allows a cue dot to appear on the screen when sequence playback is waiting for a cue. Off disables the cue dot.

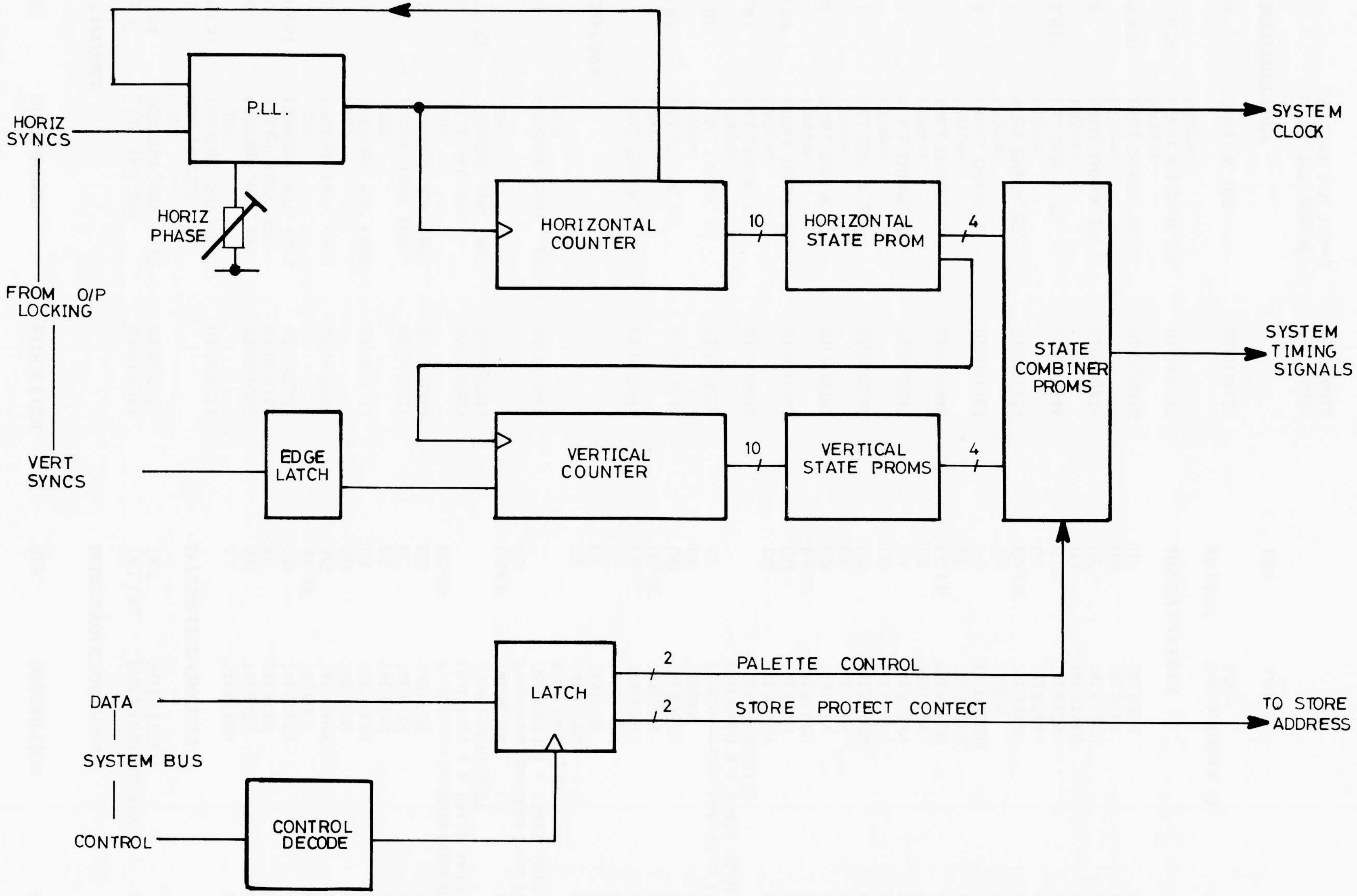
(c) Debug Mode

Setting switch HD3 on will cause the system to enter debug mode on power up or reset. This is for service engineer use only.

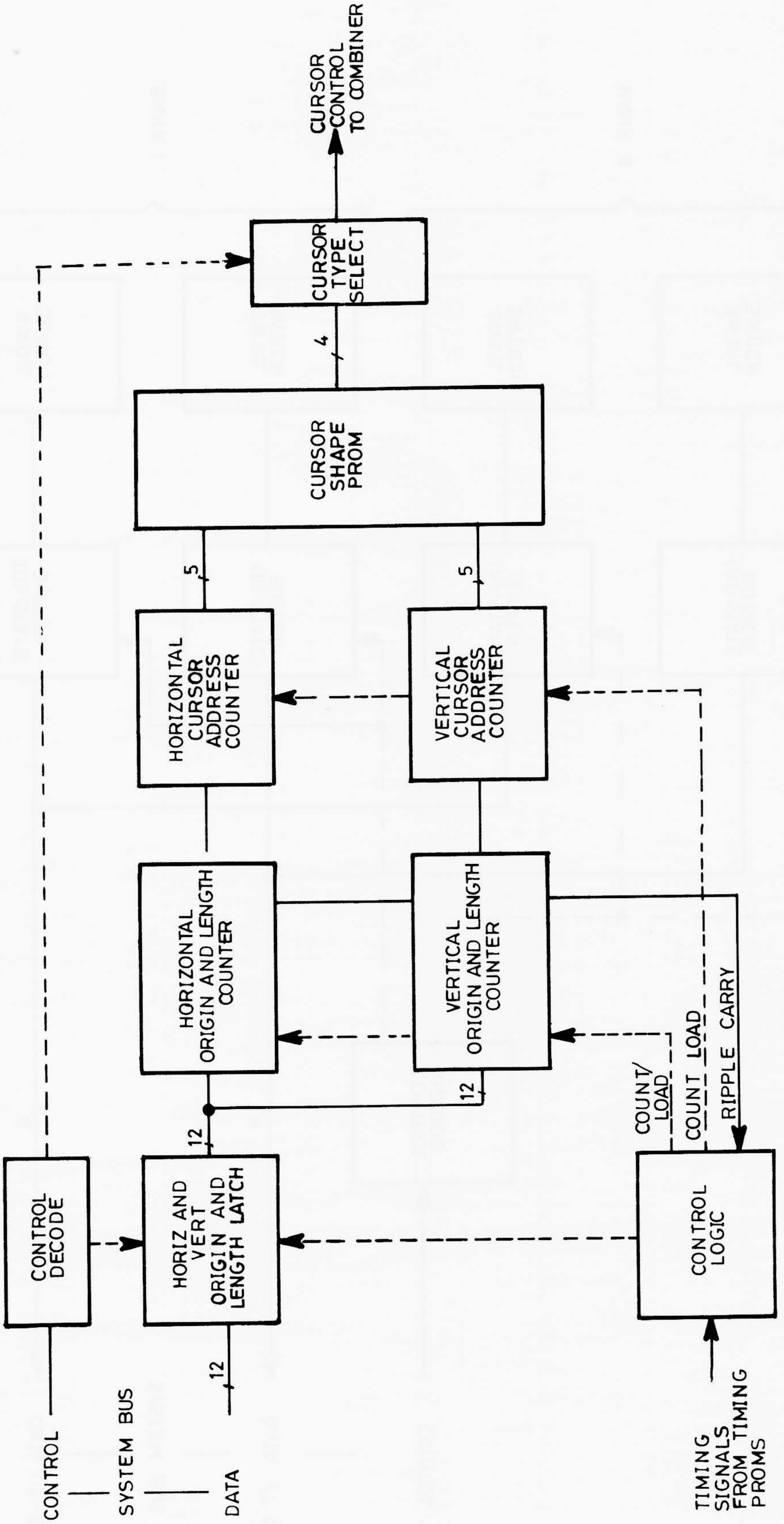
REF.	DESCRIPTION	STOCK CODE
CAPACITORS		
C1,C2	22µF, 16V, 20%	03/03/0253
C3-C54	100000pF, 50V, +80% −20%	03/06/0233
C55	NOT FITTED	
C56,C57	100000pF, 50V, +80% −20%	03/06/0233
C58	470000pF, 63V, 10%	03/05/0262
C59	2200pF, 100V, 20%	03/06/0152
C60,C61	100000pF, 50V, +80% −20%	03/0/0233
C62	10000pF, 100V, +80% −20%	03/06/0101
C63	100000pF, 50V, +80% −20%	03/06/0233
C64	1000pF, 100V, 10%	03/06/0721
C65	100000pF, 50V, +80% −20%	03/06/0233
C66	22µF, 16V, 20%	03/03/0253
C67-C70	100000pF, 50V, +80% −20%	03/06/0233
VC1	4pF-20pF, 250V, −10% +50%	03/07/0069
RESISTORS		
R1	10kΩ, 250mW, 2%, 100ppm	01/01/0948
R2,R3	1kΩ, 250mW, 2%, 100ppm	01/01/0646
R4,R5	3.3kΩ, 250mW, 2%, 100ppm	01/01/0786
R6,R7	1kΩ, 250mW, 2%, 100ppm	01/01/0646
R8,R9	100kΩ, 250mW, 2%, 100ppm	01/01/1162
R10	3.3kΩ, 250mW, 2%, 100ppm	01/01/0786
R11	1kΩ, 250mW, 2%, 100ppm	01/01/0646
R12	4.7kΩ, 250mW, 2%, 100ppm	01/01/084Y
R13	10kΩ, 250mW, 2%, 100ppm	01/01/0948
R14	100kΩ, 250mW, 2%, 100ppm	01/01/1162
R15	82kΩ, 250mW, 2%, 100ppm	01/01/1154
R16,R17	1kΩ, 250mW, 2%, 100ppm	01/01/0646
R18	5.6kΩ, 250mW, 2%, 100ppm	01/01/0875
R19,R20	10kΩ, 250mW, 2%, 100ppm	01/01/0948
R21-R24	10kΩ x 8, 125mW, 5%, 100ppm	01/08/0555
VR1	20kΩ, 1W, 10%	02/01/0127
SEMICONDUCTORS		
D1	IN916, 75V, 500mW	06/01/0083
D2	MV2107, 30V, 350mW	06/05/0018

REF.	DESCRIPTION	STOCK CODE
SEMICONDUCTORS (Cont)		
TR1,TR2	PNP ZTX212AL, 60V	05/01/0276
TR3	NOT FITTED	
INTEGRATED CIRCUITS		
AA	74LS138N	04/01/109Y
AB	74LS08N	04/01/417Y
AC	74LS74N	04/01/0728
AD	74LS153N	04/01/118X
AE,AF	74S374N	04/01/4294
AG	74LS240N	04/01/0805
AH	74S163N	04/01/370Y
BA	74LS138N	04/01/109Y
BB	74LS32N	04/01/3506
BC	74LS02N	04/01/1724
BD	74S174N	04/01/4219
BE-BG	Programmed Set Make From The Following (Ref Only) 4 x 93453 04/01/5339 1 x 6309-1 04/01/3107	
CA-CC	74LS670N	04/01/2925
CD	Programmed Set Make From The Following (Ref Only) 4 x 93453 04/01/5339 1 x 6309-1 4/01/3107	
CE	74LS175N	04/01/1457
CF	74S174N	04/01/4219
CG	74LS163N	04/01/1317
CH	74S163N	04/01/370Y
DA-DC	74S163N	04/01/370X
DD	74LS157N	04/01/1236
DE	74S04N	04/01/0167
DF	Programmed Set Make From The Folowing (Ref Only) 4 x 93453 04/01/5339 1 x 6309-1 4/01/3107	
DG	74LS163N	04/01/1317
DH	74LS74N	04/01/0728
EA-EC	74LS163N	04/01/1317
ED	74S163N	04/01/370Y
EE	74LS74N	04/01/0728
EG	74LS163N	04/01/1317
EH	74LS03PN	04/01/3085
FA	74LS138N	04/01/109Y
FB	74S163N	04/01/370Y
FC,FD	74LS163N	04/01/1317
FE	74LS221N	04/01/1589
FG	14.318MHz	28/02/0236
FH	741CN	04/01/250X
GA,GC	74LS244N	04/01/2828
GE	74LS74N	04/01/0728
GF	74LS32N	04/01/3506
HA	74LS244N	04/01/2828
HC	74LS244N	04/01/2828
HE	74LS74N	04/01/0728
HF	74LS00N	04/01/006X
MISCELLANEOUS		
SW1-SW4	Switch, 100mA, 5V, 8-Way	26/05/0049
LK1	AOT	

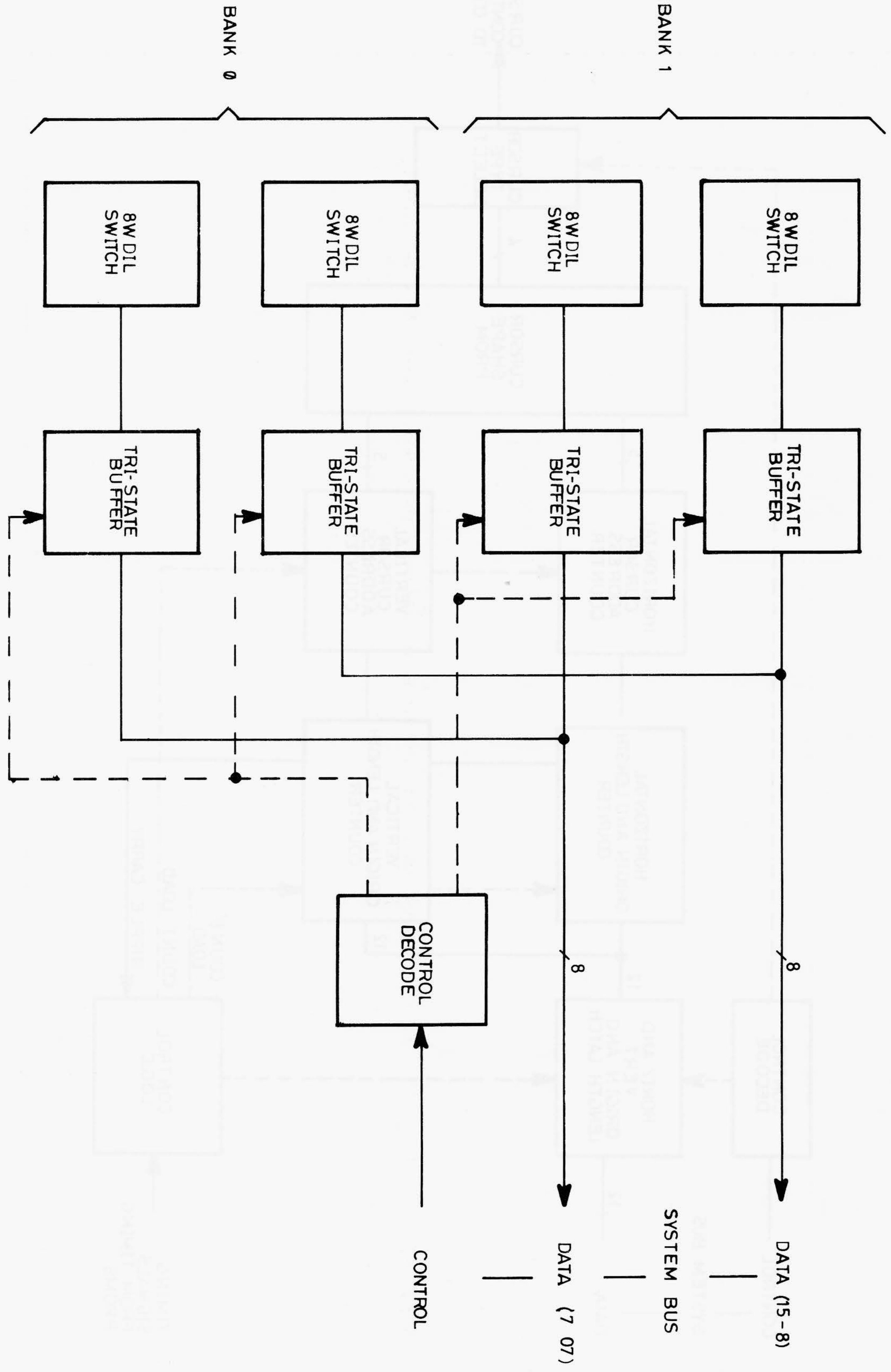
17418 Component List



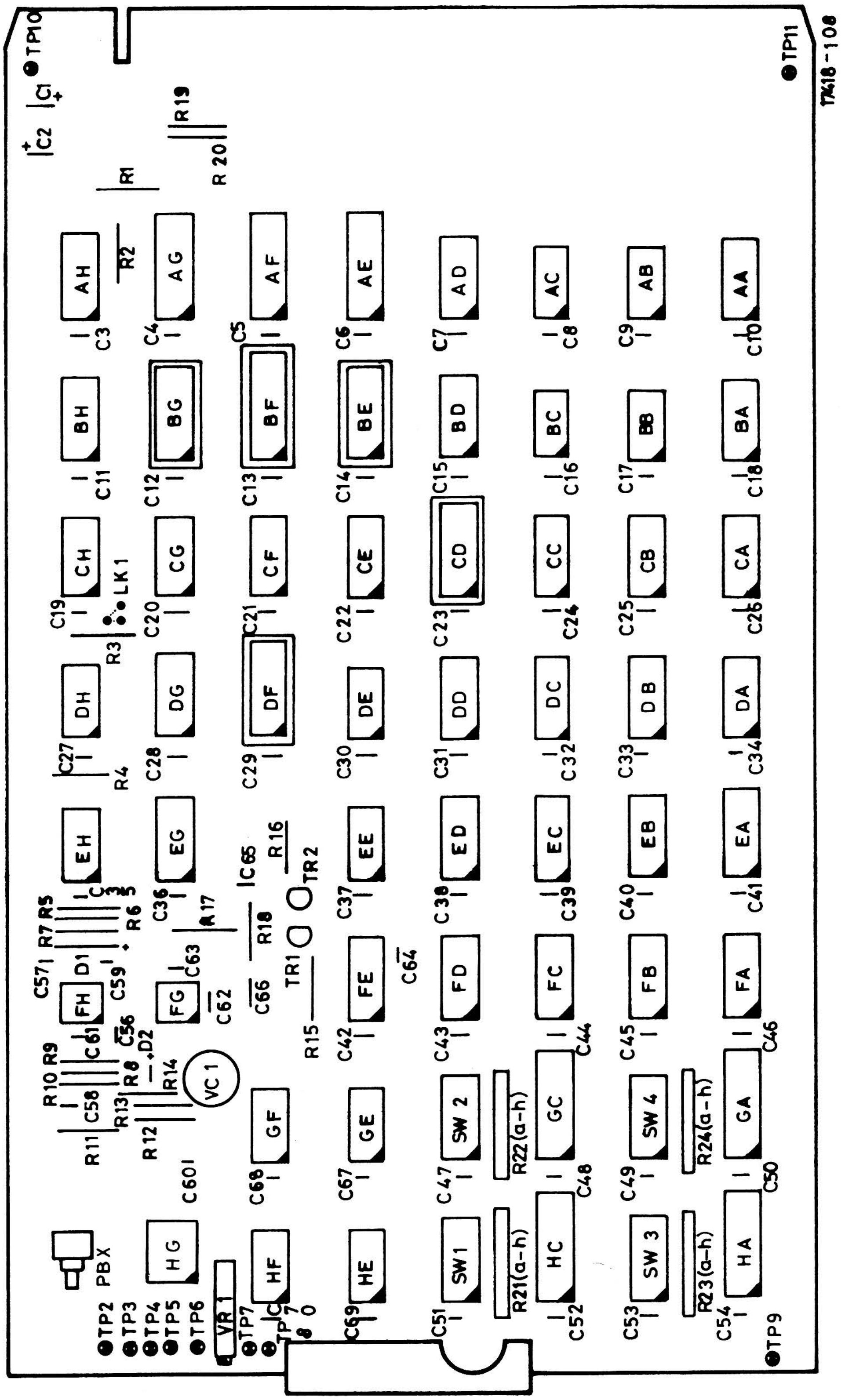
17418, Figure 1 Output Timing Card System Timing


CONTROL
SYSTEM BUS
DATA
12
CONTROL DECODE
HORIZ AND VERT ORIGIN AND LENGTH LATCH
12
12
HORIZONTAL ORIGIN AND LENGTH COUNTER
VERTICAL ORIGIN AND LENGTH COUNTER
HORIZONTAL CURSOR ADDRESS COUNTER
VERTICAL CURSOR ADDRESS COUNTER
5
5
CURSOR SHAPE PROM
4
CURSOR TYPE SELECT
CURSOR CONTROL TO COMBINER
TIMING SIGNALS FROM TIMING PROMS
CONTROL LOGIC
COUNT/LOAD
COUNT LOAD
RIPPLE CARRY

17418, Figure 2 Output Timing Card Cursor Control



17418, Figure 3 Output Timing Card Configuration Switches


T418-108
TP1
TP2
TP3
TP4
TP5
TP6
TP7
TP8
TP9
TP10
TP11
AA
AB
AC
AD
AE
AF
AG
AH
BA
BB
BC
BD
BE
BF
BG
BH
CA
CB
CC
CD
CE
CF
CG
CH
DA
DB
DC
DD
DE
DF
DG
DH
EA
EB
EC
ED
EE
EG
EH
FA
FB
FC
FD
FE
FG
FH
GA
GC
GE
GF
HA
HC
HE
HF
HG
SW 1
SW 2
SW 3
SW 4
VR 1
VC 1
PBX
LK1
TR1
TR2
D1
D2
R1
R2
R3
R4
R5
R6
R7
R8
R9
R10
R11
R12
R13
R14
R15
R16
R17
R18
R19
R 20
R21(a–h)
R22(a–h)
R23(a–h)
R24(a–h)
C1
C2
C3
C4
C5
C6
C7
C8
C9
C10
C11
C12
C13
C14
C15
C16
C17
C18
C19
C20
C21
C22
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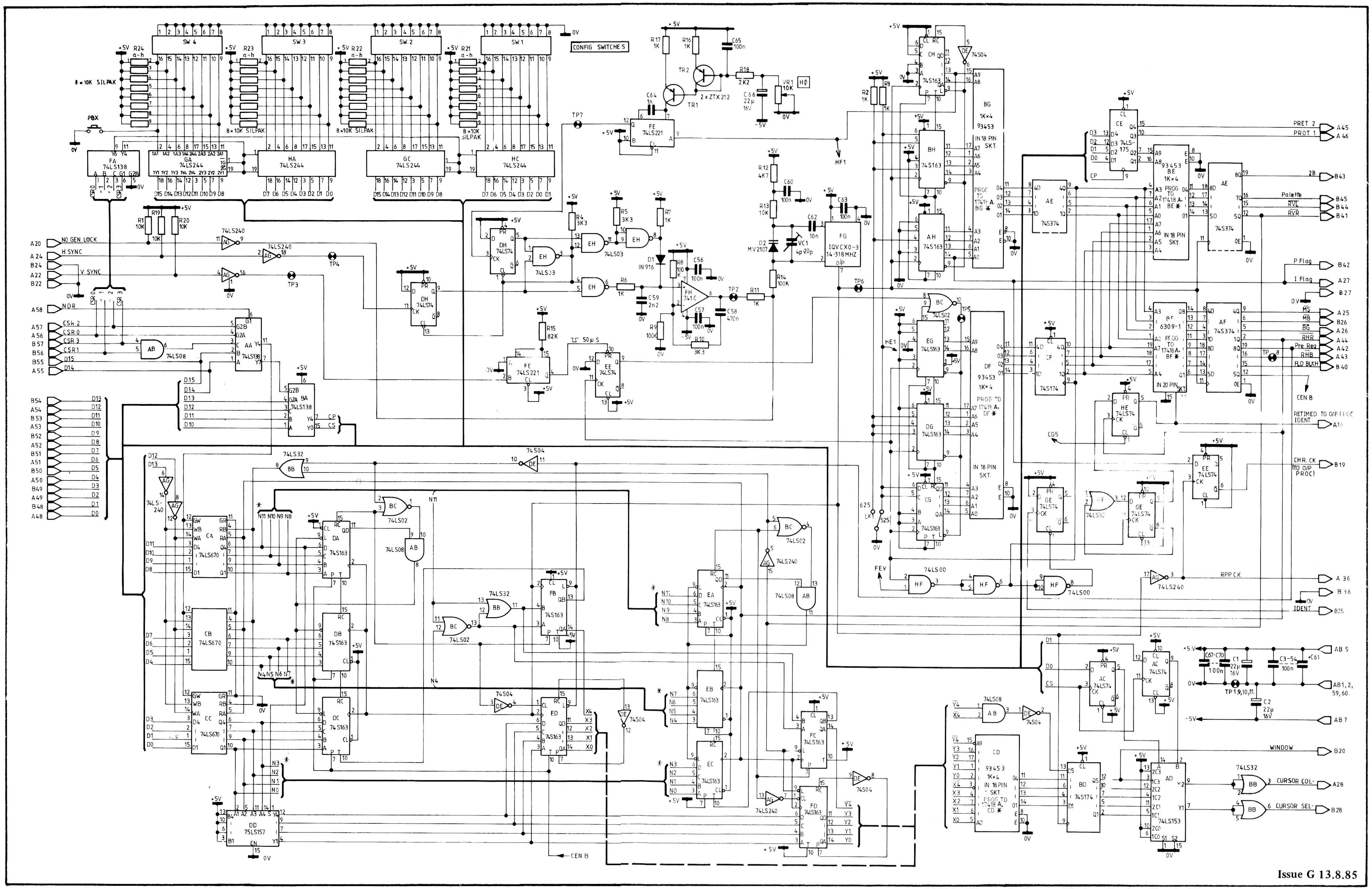

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17418, Figure 4 Output Timing Card : Circuit Diagram and Component Layout

OUTPUT LOCKING CARD

17449

1. INTRODUCTION

The Output Locking card serves two purposes:

(a) To derive syncs and burst from an external video reference.

(b) To take digital data from the tape interface and convert to a video output for recording on VTR.

2. CIRCUIT DESCRIPTION

Input reference video, preferably Black Burst, is buffered by AD and then drives two areas of the card. One demodulates burst for a phase-locked oscillator to generate subcarrier clocks for the output processor. The other stripes off syncs to generate horizontal and vertical timing signals for the line locked oscillator on the Output Timing card. This section also generates sampling pulses used by the burst-locked oscillator circuitry.

The sync signals are generated as follows.

The buffered reference signal is low pass filtered to remove most of the subcarrier and fed to CD and CE. These are configured as sample and holds and arranged to sample sync tips and black level (during burst). Their outputs are buffered by BD and added at the junction of R50 and R51 to give a level at which input syncs are sliced by comparator DD. The signal at TP7 is then TTL mixed syncs. Negative edges trigger monostable ED which gates out half line pulses of field group at FD. TP8 is then a horizontal drive signal occuring once a line (HDRIVE A24).

This signal is fed internally to JC whose use will be described later, and in inverted form as the sync tip sampling signal to CE. Further processing of this signal by FD, GD and HD generates two more timing signals - one at HD pin 4 which is a short pulse during burst period and feeds CD, the black level sampler in the sync separator, and a signal which is high for the whole of the burst period (burst gate) appearing at TP18. The mixed sync signal from TP7 is also processed by ID to give a pulse during the field group. JD uses this signal to generate a vertical sync at TP11 (V drive A26). This signal feeds BD which decides whether V drive exists and conditionally puts out a 'No Locking' signal via A20 if there are not vertical syncs. The pulse from ID also feeds through KC and JD to produce a signal which is high during field grouping where there is no burst present on the input reference video (burst blanking). This signal is logically ANDed with burst gate to provide a sampling signal which is high for burst duration, but only for lines where burst should be present on the input reference.

The following description of subcarrier phase-locking is for a PAL system, but minor differences necessary for NTSC will be noted later. The buffered reference video available at AD is fed via subcarrier bandpass filter to demodulator IC. The other input is subcarrier fed back from the output oscillator for phase comparison. The output of the demodulator is buffered, amplified and fed to sampling gates,. GB, GC and HC.

The sampling pulses for GB and GC are supplied from KD. Note that JC is clocked at line frequency, hence the outputs of Q and Q toggle at line frequency. Each output is ANDed with the burst gate signal. Thus GB and GC are fed with sampling signals active during burst gate on every other line, and the samples for GB are themselves one line out of phase with those for GC and vice versa. The two buffered samples are summed at the junction of R28 and R29, integrated and fed as an error voltage to the varicap controlling crystal oscillator EC. It is assumed that when the crystal oscillator is in phase with the subcarrier on the reference video the output of the demodulator is zero, and hence the error voltage is zero. The alternate sampling of the two sample gates is necessary because of the nature of PAL subcarrier. The output of EC is, in fact, 4 x subcarrier frequency and is fed out of the card via DB and A23. DB is a tri-state buffer which can disable the signal by SW2. Internally this signal is divided by four and fed out of the card via BC and A21. SW1 can invert the subcarrier clock passing out of the card (i.e. 180° phase shift). HC samples every line during burst, and hence is a suitable source for a PAL ident signal, and is therefore clocked at line frequency and fed out of the card via BC and A16. LK1 can invert the polarity of ident.

For NTSC links 3 and 4 are moved over such that both sampling gates receive sample pulses every line. R28 and R29 now merely average the error voltage for feeding to the crystal oscillator. Also, the ident signal is disabled and tied high with links 1 and 5. Note also that various timing components have different values or NTSC and that the subcarrier bandpass filter components are different. EC is 14.318MHz for NTSC and 17.73MHz for PAL.

The remaining section of the card is that producing the VTR output. Data comes into the card and is buffered by AB. These signals feed to CB, whose outputs control three current sources built from TR11, 12, 13 and CA. The currents are summed at the transistor collectors, passed through a filter and converted to a suitable signal level by AA and TR9 before being passed out of the card via A36 and A37 as two 75Ω feeds for a VTR.

3. IDENT

In PAL machines the Output Locking card extracts IDENT from the genlock input. IDENT is a line rate signal which is high for the first half line or for the second half line depending on which of the four fields is being viewed. IDENT can be inverted by link 1 at Exclusive-OR BC. The signal leaves the card at A16 and goes to the Output Timing card edge connector B25. The circuitry around GE on this card retimes IDENT for output H0 and also free runs if there is no feed from the Locking card (e.g. if there is no genlock). It is disabled on NTSC cards by pin 1 of HE. Retimed IDENT leaves output timing at A16 and goes to the Output Processor edge connector B25.

REF.	DESCRIPTION	STOCK CODE
CAPACITORS		
C1	100000pF, 50V, +80% −20%	03/06/0233
C2	22µF, 25V, 20%	03/03/0237
C3	100000pF, 50V, +80% −20%	03/06/0233
C4	22µF, 25V, 20%	03/03/0237
C5-C34	100000pF, 50V, +80% −20%	03/06/0233
C35	10µF, 16V, 20%	03/03/0172
C36	470000pF, 63V, 10%	03/05/0262
C37	180pF, 100V, 10%	03/06/039X
C38	33pF, 100V, 10%	03/06/0489
C39	180pF, 100V, 10%	03/06/039X
C40	NOT FITTED	
C41	100000pF, 50V, +80% −20%	03/06/0233
C42	NOT FITTED	
C43-C45	100000pF, 50V, +80% −20%	03/06/0233
C46	1000pF, 100V, 10%	03/06/0314
C47,C48	10000pF, 100V, +80% −20%	03/06/0101
C49	AOT	
C50	470000pF, 63V, 10%	03/05/0262
C51	10000pF, 100V, +80% −20%	03/06/0101
C52	8.2pF, 100V, OP5	03/06/0551
C53	10000pF, 100V, +80% −20%	03/06/0101
C54,C55	1000pF, 100V, 10%	03/06/0314
C56,C57	39pF, 100V, 10%	03/06/0039
C58	100000pF, 50V, +80% −20%	03/06/0233
C59	22µF, 25V, 20%	03/03/0237
C60	39pF, 100V, 10%	03/06/0039
C61	100000pF, 50V, +80% −20%	03/06/0233
C62	180pF, 100V, 10%	03/06/039X
C63	AOT	
C64	1000pF, 100V, 10%	03/06/0314
C65	10000pF, 100V, +80% −20%	03/06/0101
C66	10000pF, 63V, 10%	03/05/0319
C67	220pF, 100V, 10%	03/06/0055
C68	150pF, 100V, 10%	03/06/0365
C69	270pF, 100V, 10%	03/06/0349
C70	1000pF, 100V, 10%	03/06/0314
C71	330pF, 100V, 10%	03/06/0373
C72	10000pF, 63V, 10%	03/05/0319
C73	NOT FITTED	
C74	330pF, 100V, 10%	03/06/0373
C75	100000pF, 50V, +80% −20%	03/06/0233
C76	100000pF, 63V, 10%	03/05/0289
C77	220000pF, 63V, 10%	03/05/027Y
C78	100000pF, 63V, 10%	03/05/0289
C79	100000pF, 50V, +80% −20%	03/06/0233
C80,C81	10000pF, 100V, +80% −20%	03/06/0101
C82	100000pF, 50V, +80% −20%	03/06/0233
C83	100000pF, 63V, 10%	03/05/0289
C84	330pF, 100V, 10%	03/06/0373
C85	68pF, 100V, 10%	03/06/0497
C86	100000pF, 50V, +80% −20%	03/06/0233
C87	10000pF, 100V, +80% −20%	03/06/0101
C88	470000pF, 63V, 10%	03/05/0262
C89,C90	22µF, 25V, 20%	03/03/0237
C91,C92	100000pF, 50V, +80% −20%	03/06/0233
C93	68pF, 100V, 10%	03/06/0497
C94	NOT FITTED	
C95	6.8µF, 25V, 20%	03/03/0148
CAPACITORS (Cont.)		
C96	100000pF, 50V, +80% −20%	03/06/0233
C97-C99	NOT FITTED	
C100,C101	100000pF, 50V, +80% −20%	03/06/0233
VC1	3.5pF-25, 50V	03/07/0212
RESISTORS		
R1	NOT FITTED	
R2	1MΩ, 330mW, 5%, 250ppm	01/01/1332
R3-R5	470Ω, 250mW, 2%, 100ppm	01/01/0557
R6,R7	2.2kΩ, 250mW, 2%, 100ppm	01/01/1642
R8,R9	3.9kΩ, 250mW, 2%, 100ppm	01/01/0808
R10,R11	200Ω, 250mW, 2%, 100ppm	01/01/0425
R12,R13	2.2kΩ, 250mW, 2%, 100ppm	01/01/1642
R14	820Ω, 250mW, 1%, 50ppm	01/01/0611
R15,R16	12kΩ, 250mW, 2%, 100ppm	01/01/0964
R17	22kΩ, 250mW, 2%, 100ppm	01/01/1014
R18	4.7kΩ, 250mW, 2%, 100ppm	01/01/084Y
R19	5.1kΩ, 250mW, 2%, 100ppm	01/01/0867
R20	12kΩ, 250mW, 2%, 100ppm	01/01/0964
R21	4.3kΩ, 250mW, 2%,	01/01/0832
R22	5.1kΩ, 250mW, 2%, 100ppm	01/01/0867
R23	12kΩ, 250mW, 2%, 100ppm	01/01/0964
R24	4.3kΩ, 250mW, 2%, 100ppm	01/01/0832
R25	5.1kΩ, 250mW, 2%, 100ppm	01/01/0867
R26,R27	1kΩ, 250mW, 2%,	01/01/0646
R28,R29	10kΩ, 250mW, 2%, 100ppm	01/01/0948
R30	1kΩ, 250mW, 2%, 100ppm	01/01/0646
R31	3.3kΩ, 250mW, 2%, 100ppm	01/01/0786
R32	100kΩ, 250mW, 2%, 100ppm	01/01/1162
R33,R34	4.7kΩ, 250mW, 2%, 100ppm	01/01/084Y
R35-R37	1kΩ, 250mW, 2%, 100ppm	01/01/0646
R38	4.7kΩ, 250mW, 2%, 100ppm	01/01/084Y
R39,R40	680Ω, 250mW, 2%, 100ppm	01/01/059X
R41	2.2kΩ, 250mW, 2%, 100ppm	01/01/1642
R42	1.8kΩ, 250mW, 2%, 100ppm	01/01/070Y
R43	560Ω, 250mW, 2%, 100ppm	01/01/0581
R44	15kΩ, 250mW, 2%, 100ppm	01/01/0972
R45	680Ω, 250mW, 2%, 100ppm	01/01/059X
R46	1kΩ, 250mW, 2%, 100ppm	01/01/0646
R47	4.7MΩ, 330mW, 5%, 250ppm	01/01/1383
R48	1MΩ, 330mW, 5%, 250ppm	01/01/1332

17449 Component List

RESISTORS (Cont.)

REF.	DESCRIPTION	STOCK CODE
R49	2.2kΩ, 250mW, 2%, 100ppm	01/01/1642
R50,R51	4.7kΩ, 250mW, 2%, 100ppm	01/01/084Y
R52	1kΩ, 250mW, 2%, 100ppm	01/01/0646
R53	7.5kΩ, 250mW, 2%, 100ppm	01/01/0913
R54	100Ω, 250mW, 2%, 100ppm	01/01/0336
R55	4.7kΩ, 250mW, 2%, 100ppm	01/01/084Y
R56	27kΩ, 250mW, 2%, 100ppm	01/01/103Y
R57	5.6kΩ, 250mW, 2%, 100ppm	01/01/0875
R58	9.09kΩ, 250mW, 1%, 50ppm	01/01/2185
R59	10kΩ, 250mW, 2%, 100ppm	01/01/0948
R60	15kΩ, 250mW, 2%, 100ppm	01/01/0972
R61	10kΩ, 250mW, 2%, 100ppm	01/01/0948
R62	15kΩ, 250mW, 2%, 100ppm	01/01/0972
R63	1kΩ, 250mW, 2%, 100ppm	01/01/0646
R64	20kΩ, 250mW, 2%, 100ppm	01/01/1952
R65	10kΩ, 250mW, 2%, 100ppm	01/01/0948
R66	1kΩ, 250mW, 2%, 100ppm	01/01/0646
R67	100kΩ, 250mW, 2%, 100ppm	01/01/1162
R68	5.6kΩ, 250mW, 2%, 100ppm	01/01/0875
R69	10kΩ, 250mW, 2%, 100ppm	01/01/0948
R70	100kΩ, 250mW, 2%, 100ppm	01/01/1162
R71	47kΩ, 250mW, 2%, 100ppm	01/01/1103
R72	12kΩ, 250mW, 2%, 100ppm	01/01/0964
R73	1kΩ, 250mW, 2%, 100ppm	01/01/0646
R74	8.2kΩ, 250mW, 2%, 100ppm	01/01/0921
R75,R76	9.1kΩ, 250mW, 2%, 100ppm	01/01/093X
R77	22kΩ, 250mW, 2%, 100ppm	01/01/1014
R78	2.7kΩ, 250mW, 2%, 100ppm	01/01/0743
R79	820Ω, 250mW, 1%, 50ppm	01/01/0611
R80	1.2kΩ, 250mW, 2%, 100ppm	01/01/0662
R81	2.7kΩ, 250mW, 2%, 100ppm	01/01/0743
R82	1.8kΩ, 250mW, 2%, 100ppm	01/01/070Y
R83	2.7kΩ, 250mW, 2%, 100ppm	01/01/0743
R84	200Ω, 250mW, 2%, 100ppm	01/01/0425
R85	560Ω, 250mW, 2%, 100ppm	01/01/0581
R86	470Ω, 250mW, 2%, 100ppm	01/01/0557
R87	8.2kΩ, 250mW, 2%, 100ppm	01/01/0921
R88,R89	10kΩ, 250mW, 2%, 100ppm	01/01/0948

RESISTORS (Cont.)

REF.	DESCRIPTION	STOCK CODE
R90,R91	1kΩ, 250mW, 2%, 100ppm	01/01/0646
R92	470Ω, 250mW, 2%, 100ppm	01/01/0557
R93	330Ω, 250mW, 2%, 100ppm	01/01/1723
R94	820Ω, 250mW, 1%, 50ppm	01/01/0611
R95,R96	75Ω, 250mW, 2%, 100ppm	01/01/0263
R97	1.2kΩ, 250mW, 2%, 100ppm	01/01/0662
R98	100kΩ, 250mW, 2%, 100ppm	01/01/1162
R99	1.2kΩ, 250mW, 2%, 100ppm	01/01/0662
R100	4.7kΩ, 250mW, 2%, 100ppm	01/01/084Y
VR1	200Ω, 500mW, 10%	02/02/0025
VR2	2kΩ, 500mW, 10%	02/02/005X
VR3	5kΩ, 500mW, 10%	02/03/0047
VR4	NOT FITTED	
VR5	5kΩ, 500mW, 10%	02/02/0068
VR6	50kΩ, 500mW, 10%	02/02/0092

SEMICONDUCTORS

REF.	DESCRIPTION	STOCK CODE
D1-D3	IN916, 75V	06/01/0083
D4	MV2107, 30V	06/05/0018
D5	TA 50822835	06/01/0075
D6	NOT FITTED	
D7,D8	TA OA47, 25V	06/01/021Y
D9-D12	NOT FITTED	
D13,D14	IN4148, 75V	06/01/0105
TR1-TR5	PNP BC309C, 45V	05/01/0454
TR6-TR8	NPN BC239C, 45V	05/01/0446
TR9	NPN 2N2219, 60V	05/01/0039
TR10-TR13	PNP BC309C, 45V	05/01/0454
TR14,TR15	NPN BC239C, 45V	05/01/0446

INTEGRATED CIRCUITS

REF.	DESCRIPTION	STOCK CODE
AA	LIN 3507J	04/02/012X
AB	74LS240N	04/01/2879
AC	74LS244N	04/01/2828
AD	LIN 0033CG	04/02/0111
BB	74LS74N	04/01/0728
BC	74LS86N	04/01/0833
BD	LIN 4605-1	04/03/1598
CA	LIN 348N	04/01/2674
CB	74LS03PN	04/01/3085
CC	74LS113N	04/01/5029
CD,CE	LIN 3080E	04/03/3043
DB	74LS244N	04/01/2828
DC	74331N	04/01/157Y
DD	LIN 311N	04/03/3604
EC	14.318MHz	28/02/0236
ED	1010E	04/01/2518
FC	LIN 4605-5	04/03/1598
FD	74LS221N	04/01/1589
GB,GC	LIN 3080E	04/03/3043
GD	74LS74N	04/01/0728
HB	LIN 311N	04/03/3604
HC	LIN 3080E	04/03/3043
HD	74221N	04/01/157Y
IC	LIN 1495L	04/01/1902
ID	LIN 311N	04/03/3604
JC	74LS74N	04/01/0728
JD-KC	74LS221N	04/01/1589
KD	74LS08N	04/01/417Y

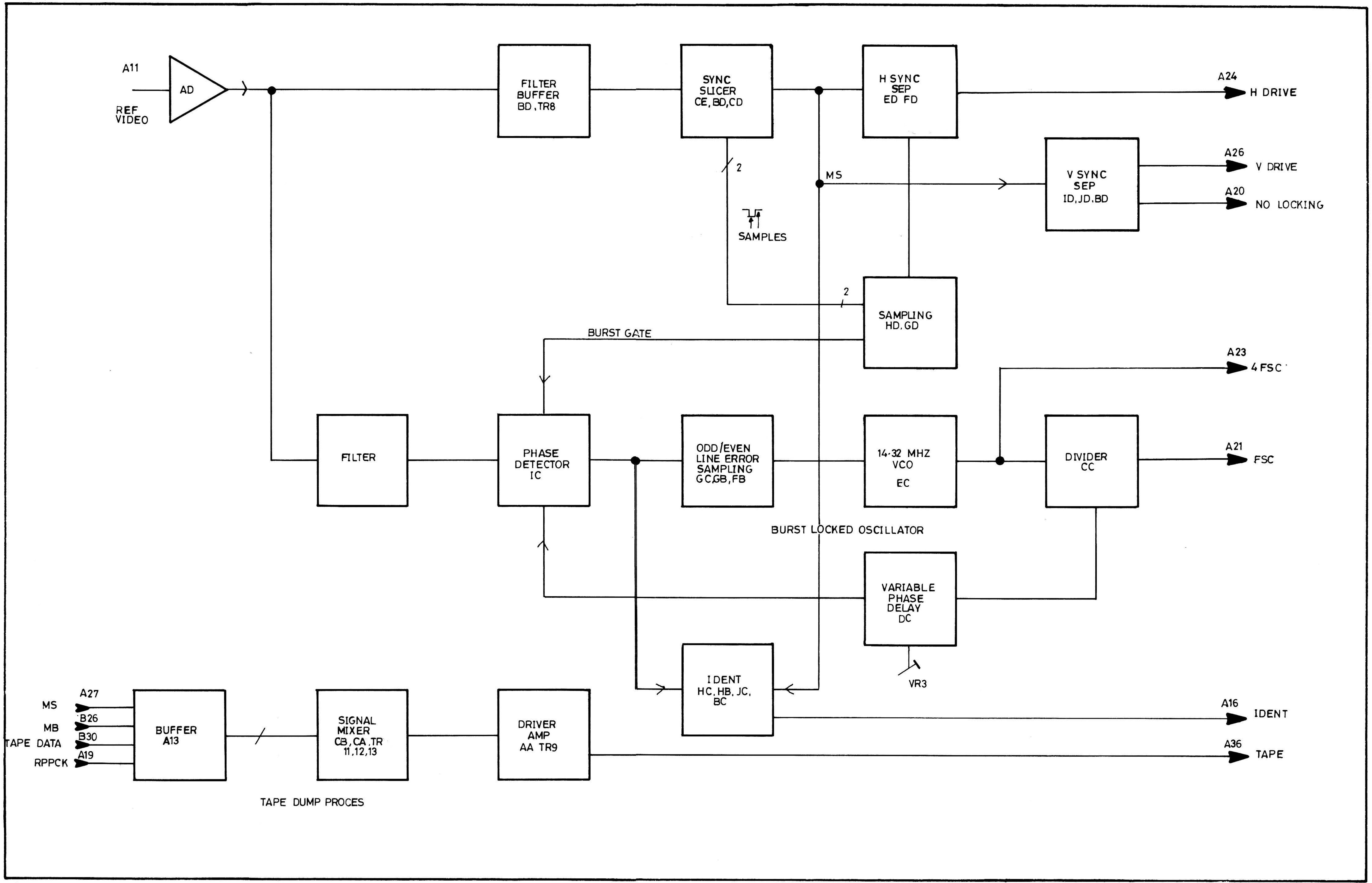
MISCELLANEOUS

REF.	DESCRIPTION	STOCK CODE
L1,L2	Link	07/01/0087

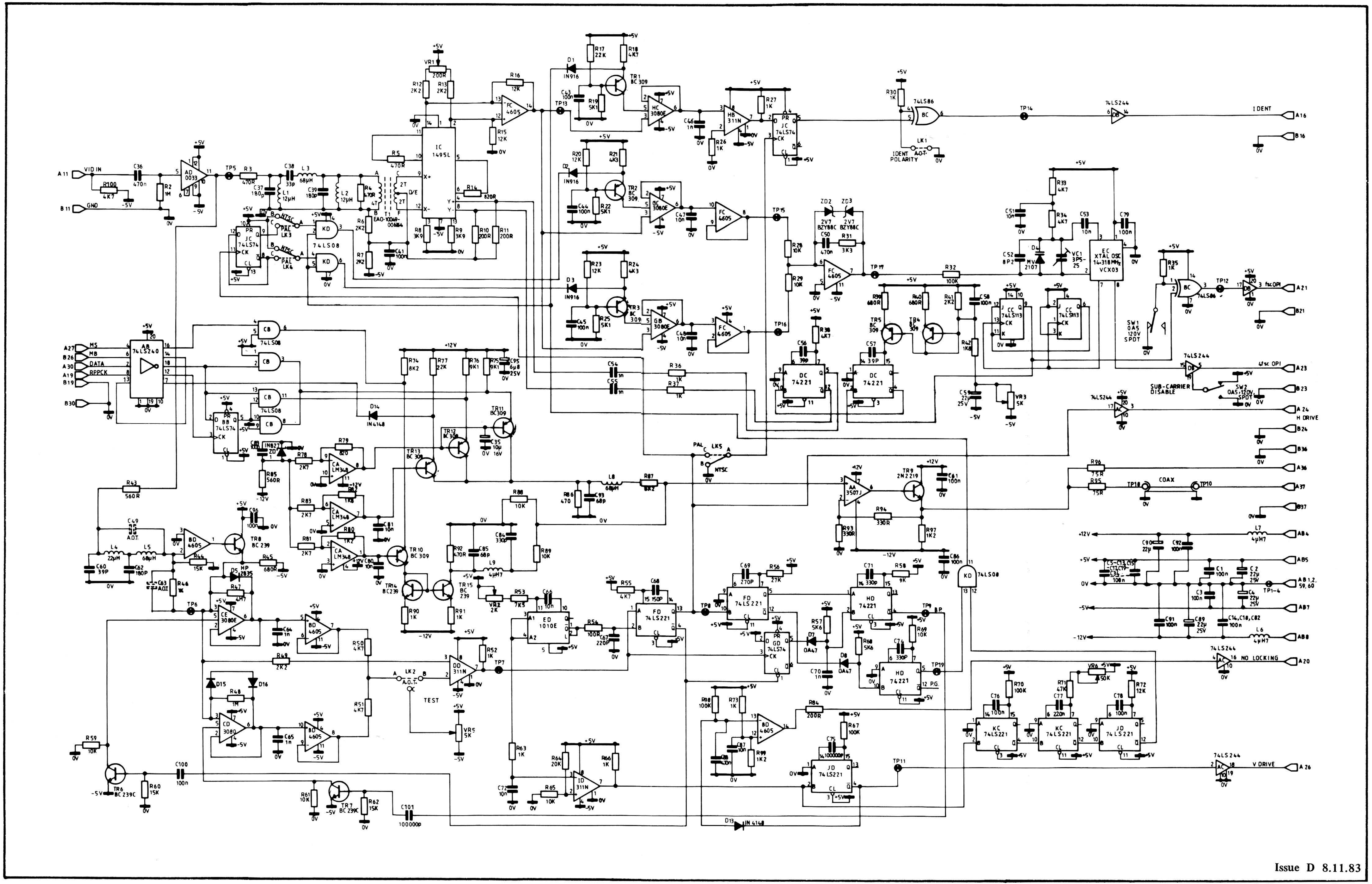
17449 Component List (Cont.)

REF.	DESCRIPTION	STOCK CODE
MISCELLANEOUS		
L3	68μH, 215MA, 10%	07/01/0168
L4	22μH, 265MA, 10%	07/01/0125
L5	68μH, 215MA, 10%	07/01/0168
L6,L7	4.7μH, 260MA, 10%	07/01/0052
L8	68μH, 215MA, 10%	07/01/0168
L9	4.7μH, 260MA, 10%	07/01/0052
SW1,SW2	Switch, 120V	26/02/0085
LK1-LK5	1MM, FLD HIGHPROF 2.25 HOLE BLIND 0314 450-366-01-03-00	

17449 Component List (Cont.)



17449, Figure 1 Output Locking Card Block Diagram



17449, Figure 2 Output Locking Card : Circuit Diagram and Component Layout

INPUT LOCKING CARD

17564

1. INTRODUCTION

The Input Locking card performs three functions shown on the block diagram, namely sync separation, video clamping and data reconstruction for the tape interface. The three inputs to the card, RGB syncs, composite video and data are routed to the appropriate parts of the card by the FET switch AG under computer control from a register on the Input Timing card 17447 as shown in Table 1. AG contains four independent switches (A, B, C, D) with control inputs. Input low = switch on.

A35 VTR	A27 RGB	Select Source	Destinations
0	0	Composite Video	Clamp, Sync Sep
0	1	RGB Syncs	Sync Sep
1	X	Tape Data	Sync Sep., Data Slicer

2. SYNC SEPARATOR

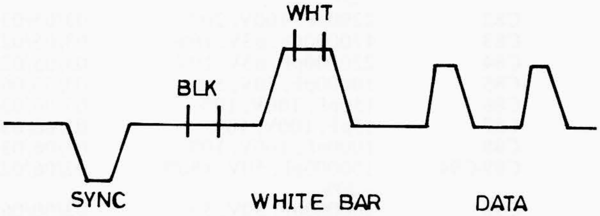
Video from the selected source is low pass filtered and buffered by DF and TR3 to remove noise and subcarrier before being fed to the adaptive sync slicer. OTA DE samples sync bottoms by means of a sample pulse derived from the monostable chain that follows the comparator EF. Start-up is ensured by diode D1, R15 and R16 which make the adaptive slice level sit half way up syncs in the absence of sample pulses. Similary CF samples during the back porch, its sample period being long enough to completely cover colour burst. In normal operation the buffered outputs of the samples are then averaged by R20, R21 to give the mid point of syncs before being fed to the reference input of comparator EF. To simplify testing of the circuit LK1 allows a fixed slice level to be set by VR1. This should be set, with LK1 in the A B position, to make the voltage on pin 2 of EG midway up syncs as seen on pin 3 of EG. A chain of monostables follows the comparator EF to provide the sample and clamp pulse required by the remainder of the card. The only essential adjustment required here is VR2, which should be set so that there is only one line sync pulse per line during field group at pin 13 of FF.

3. VIDEO CLAMP

Composite video is amplified by BG and has d.c. offset added from AE pin 8 via R48. This d.c. offset is generated by sample gate BF and integrator AE pins 5, 6, 7 such that the black level of the video at TP16 is 0V. As with the sync slicer, the sample pulse completely covers colour burst.

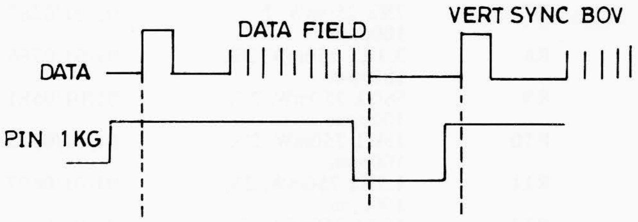
4. DATA SLICER

Serial picture data from the digital input is first filtered to remove any subcarrier which may be present if a tape recorder is used in 'colour' mode. (It is recommended that all tape dumps/loads should be performed with the tape recorder in monochrome mode.) Amplifier CC restores the data to its original amplitude to drive the adaptive slicer and comparator. The adaptive data slicer DC and EC samples the data stream to determine the set-up black level (low) and the white (high) level. The positions of the sample pulses are adjustable, VR6 being the black sample position, set to be on the portion of set-up prior to the white bar on each line, and VR5, the white sample positions which is set to sample in the centre of the white bar.



Positions of Sample Pulses

To prevent the data sample level drifting during field group when there are no white bars to sample, the white sample pulse is gated off by field lock-out monostables KF and LF. The position of the blanking pulse being set by VR7 to cover the period when the white bar is absent. For testing, LK4 allows a fixed slice level to be set on VR4.



REF.	DESCRIPTION	STOCK CODE
CAPACITORS		
C1-C4	100000pF, 50V, +80% −20%	03/06/0233
C5-C9	22μF, 25V, 20%	03/03/0237
C10	470000pF, 63V, 10%	03/05/0262
C11	39pF, 100V, 10%	03/06/0039
C12	180pF, 100V, 10%	03/06/039X
C13-C15	100000pF, 50V, +80% −20%	03/06/0233
C16,C17	1000pF, 100V, 10%	03/06/0314
C18,C19	220pF, 100V, 10%	03/06/0055
C20,C21	10000pF, 63V, 10%	03/05/0319
C22	270pF, 100V, 10%	03/06/0349
C23	470pF, 100V, 10%	03/06/0241
C24	1000pF, 100V, 10%	03/06/0314
C25	10000pF, 63V, 10%	03/05/0319
C26	270pF, 100V, 10%	03/06/0349
C27	470pF, 100V, 10%	03/06/0241
C28	1000pF, 100V, 10%	03/06/0314
C29	220000pF, 63V, 10%	03/05/027Y
C30	NOT FITTED	
C31	27pF, 100V, 10%	03/06/047Y
C32,C33	10000pF, 100V, +80% −20%	03/06/0101
C34	470000pF, 63V 10%	03/05/0262
C35	330pF, 100V, 10%	03/06/0373
C36	82pF, 100V, 10%	03/01/021X
C37,C38	180pF, 100V, 10%	03/06/039X
C39	82pF, 100V, 10%	03/01/021X
C40,C41	180pF, 100V, 10%	03/06/039X
C42,C43	10000pF, 100V, +80% −20%	03/06/0101
C44-C81	100000pF, 50V, +80% −20%	03/06/0233
C82	2200pF, 100V, 20%	03/05/0394
C83	470000pF, 63V, 10%	03/05/0262
C84	220000pF, 63V, 10%	03/05/027Y
C85	10000pF, 50V, 5%	03/00/0656
C86	150pF, 100V, 10%	03/06/0365
C87	15pF, 100V, 10%	03/06/033Y
C88	1000pF, 100V, 10%	03/06/0314
C89-C94	100000pF, 50V, +80% −20%	02/06/0233
C95	100000pF, 50V, 5%	03/00/0656
C96	220000pF, 63V, 10%	03/05/027Y
RESISTORS		
R1	75Ω, 250mW, 2%, 100ppm	01/01/0263
R2	1MΩ, 330mW, 5%, 250ppm	01/01/1332
R3	75Ω, 250mW, 2%, 100ppm	01/01/0263
R4,R5	470Ω, 250mW, 2%, 100ppm	01/01/0557
R6	82Ω, 250mW, 2%, 100ppm	01/01/0271
R7	75Ω, 250mW, 2%, 100ppm	01/01/0263
R8	3.3kΩ, 250mW, 2%, 100ppm	01/01/0786
R9	560Ω, 250mW, 2%, 100ppm	01/01/0581
R10	15kΩ, 250mW, 2%, 100ppm	01/01/0972
R11	1.5kΩ, 250mW, 2%, 100ppm	01/01/0697
R12	10kΩ, 250mW, 2%, 100ppm	01/01/0948
R13	680Ω, 250mW, 2%, 100ppm	01/01/059X
R14	15kΩ, 250mW, 2%, 100ppm	01/01/0972
R15	4.7MΩ, 250mW, 2%, 100ppm	01/01/1383
R16	1MΩ, 330mW, 5%, 250ppm	01/01/1332

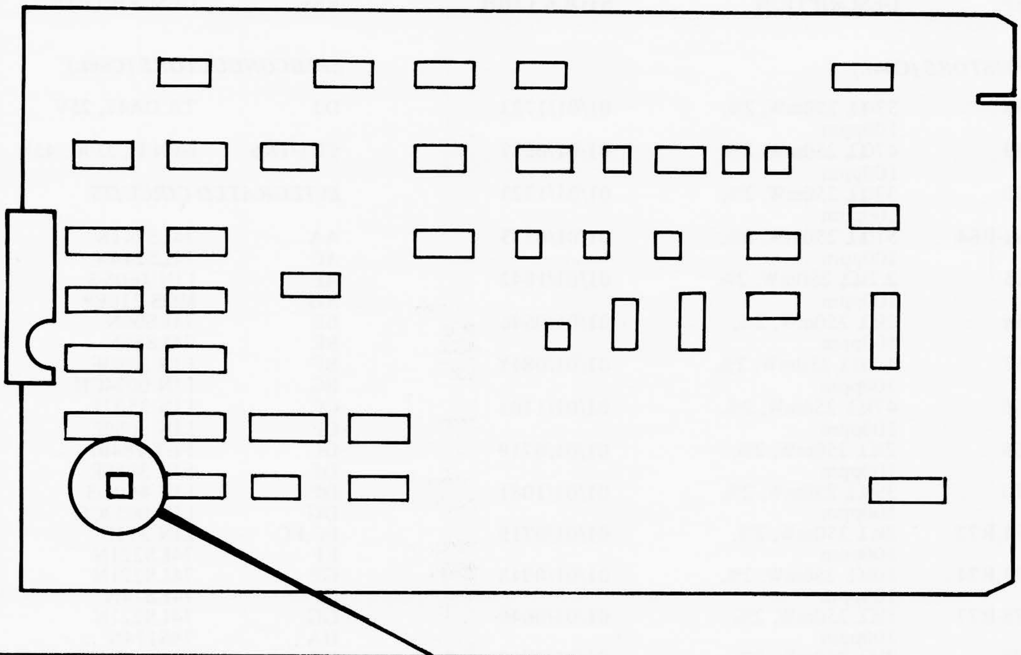
REF.	DESCRIPTION	STOCK CODE
RESISTORS (Cont.)		
R17	10kΩ, 250mW, 2%, 100ppm	01/01/0948
R18	15kΩ, 250mW, 2%, 100ppm	01/01/0972
R19	2.2kΩ, 250mW, 2%, 100ppm	01/01/1642
R20,R21	4.7kΩ, 250mW, 2%, 100ppm	01/01/084Y
R22	10kΩ, 250mW, 2%, 100ppm	01/01/0948
R23	1kΩ, 250mW, 2%, 100ppm	01/01/0646
R24,R25	10kΩ, 250mW, 2%, 100ppm	01/01/0948
R26	8.2kΩ, 250mW, 2%, 100ppm	01/01/0921
R27	18kΩ, 250mW, 2%, 100ppm	01/01/1006
R28	10kΩ, 250mW, 2%, 100ppm	01/01/0948
R29	1kΩ, 250mW, 2%, 100ppm	01/01/0646
R30	2kΩ, 250mW, 2%, 100ppm	01/01/0719
R31	1kΩ, 250mW, 2%, 100ppm	01/01/0646
R32	5.6kΩ, 250mW, 2%, 100ppm	01/01/0875
R33	47kΩ, 250mW, 2%, 100ppm	01/01/1103
R34	27kΩ, 250mW, 2%, 100ppm	01/01/103Y
R35	5.6kΩ, 250mW, 2%, 100ppm	01/01/0875
R36	1.8kΩ, 250mW, 2%, 100ppm	01/01/070Y
R37	22kΩ, 250mW, 2%, 100ppm	01/01/1014
R38	1kΩ, 250mW, 2%, 100ppm	01/01/0646
R39	6.2kΩ, 250mW, 2%, 100ppm	01/01/0891
R40	1kΩ, 250mW, 2%, 100ppm	01/01/0646
R41	100kΩ, 240mW, 2%, 100ppm	01/01/1162
R42	1kΩ, 250mW, 2%, 100ppm	01/01/0646
R43	4.7kΩ, 250mW, 2%, 100ppm	01/01/084Y
R44	470kΩ, 250mW, 2%, 100ppm	01/01/179Y
R45	1kΩ, 250mW, 2%, 100ppm	01/01/0646
R46	270Ω, 250mW, 2%, 100ppm	01/01/0476
R47	470Ω, 250mW, 2%, 100ppm	01/01/0557
R48	1kΩ, 250mW, 2%, 100ppm	01/01/0646
R49	27kΩ, 250mW, 2%, 100ppm	01/01/103Y
R50	75Ω, 250mW, 2%, 100ppm	01/01/0263
R51	33kΩ, 250mW, 2%, 100ppm	01/01/1065
R52	10kΩ, 250mW, 2%, 100ppm	01/01/0948
R53	8.2kΩ, 250mW, 2%, 100ppm	01/01/0921
R54	3.3kΩ, 250mW, 2%, 100ppm	01/01/0786
R55,R56	1kΩ, 250mW, 2%, 100ppm	01/01/0646
R57	470Ω, 250mW, 2%, 100ppm	01/01/0557

17564 Component List

REF.	DESCRIPTION	STOCK CODE
RESISTORS (Cont.)		
R58	330Ω, 250mW, 2%, 100ppm	01/01/1723
R59	470Ω, 250mW, 2%, 100ppm	01/01/0557
R60	330Ω, 250mW, 2%, 100ppm	01/01/1723
R61-R64	510Ω, 250mW, 2%, 100ppm	01/01/0573
R65	2.2kΩ, 250mW, 2%, 100ppm	01/01/1642
R66	1kΩ, 250mW, 2%, 100ppm	01/01/0646
R67	4.7kΩ, 250mW, 2%, 100ppm	01/01/084Y
R68	47kΩ, 250mW, 2%, 100ppm	01/01/1103
R69	2kΩ, 250mW, 2%, 100ppm	01/01/0719
R70	39kΩ, 250mW, 2%, 100ppm	01/01/1081
R71,R72	2kΩ, 250mW, 2%, 100ppm	01/01/0719
R73,R74	10kΩ, 250mW, 2%, 100ppm	01/01/0948
R75-R77	1kΩ, 250mW, 2%, 100ppm	01/01/0646
R78	2kΩ, 250mW, 2%, 100ppm	01/01/0719
R79	4k%, 250mW, 2%, 100ppm	01/01/0816
R80	8.2kΩ, 250mW, 2%, 100ppm	01/01/0921
R81	1kΩ, 250mW, 2%, 100ppm	01/01/0646
R82	220Ω, 250mW, 2%, 100ppm	01/01/0441
R83,R84	10kΩ, 250mW, 2%, 100ppm	01/01/0948
R85	1kΩ, 250mW, 2%, 100ppm	01/01/0646
R86	2.2kΩ, 250mW, 2%, 100ppm	01/01/1642
R87	33kΩ, 250mW, 2%, 100ppm	01/01/1065
VR1	5kΩ, 250mW, 2%, 10%	02/02/0068
VR2,VR3	2kΩ, 500mW, 10%	02/02/005X
VR4-VR6	5kΩ, 500mW, 10%	02/02/0068
VR7	50kΩ, 500mW, 10%	02/02/0092
VR8	5kΩ, 500mW, 10%	02/02/0068
SEMICONDUCTORS		
D1	TA 50822835, 5V	06/01/0075

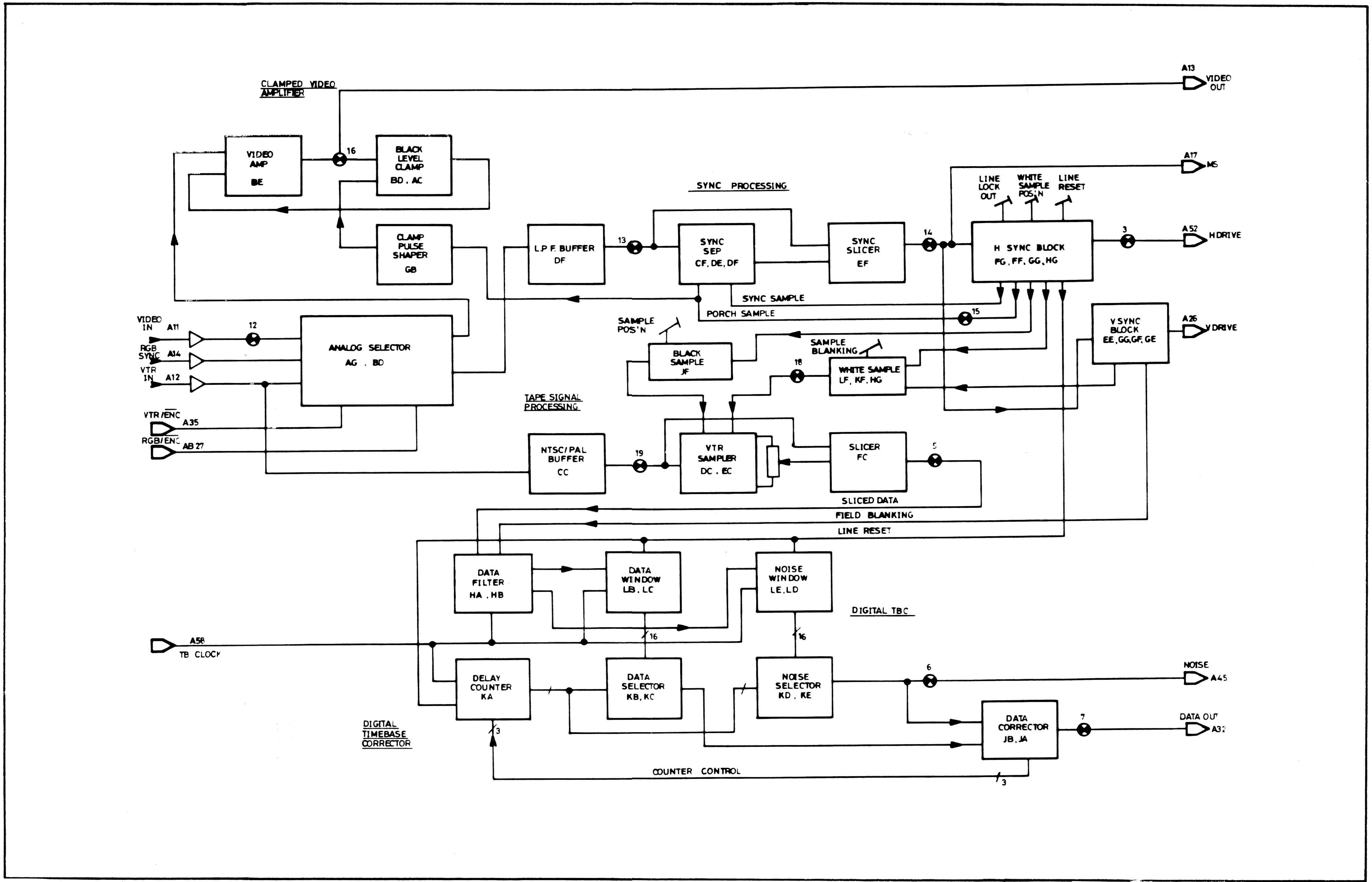
REF.	DESCRIPTION	STOCK CODE
SEMICONDUCTORS (Cont.)		
D2	TA OA47, 25V	06/01/021Y
TR1-TR6	NPN BC239C, 45V	05/01/0446
INTEGRATED CIRCUITS		
AA	74LS241N	04/01/3808
AC	74LS244N	04/01/2828
AE	LIN 4605-5	04/03/1598
AG	MOS 210BP	04/02/0383
BD	74LS00N	04/01/006X
BE	74LS86N	04/01/0833
BF	LIN 3080E	04/03/3043
BG	LIN 0024CH	04/02/1013
CC	LIN 3507J	04/02/012X
CF	LIN 3080E	04/03/3043
DC	FET 184BP	04/01/4111
DE	LIN 3080E	04/03/3043
DF	LIN 4605-5	04/03/1598
DG	LIN 0033CG	04/02/0111
FC,FC	LIN 311N	04/03/3604
FF	74LS221N	04/01/1589
GE	74LS221N	04/01/1589
GF	74LS74N	04/01/0728
GG	74LS221N	04/01/1589
HA	74S174N	04/01/4219
HB	PROM SET MAKE FROM 1 x 04/01/8532 27S21 DC 1 x 04/01/7811 PAL 16R6ACN	
HG	74LS221N	04/01/1589
JA	74S00n	04/01/0035
JB	PROM SET MAKE FROM 1 x 04/01/8532 27S21 DC 1 x 04/01/7811 PAL 16R6ACN	
JE,JF	74LS221N	04/01/1589
KA	74S169N	04/01/1368
KB-KE	74S251N	04/01/6394
KG	74LS08N	04/01/417Y
LA	100MA, 5V	26/05/0081
LB-LE	74S299N	04/01/6025
MISCELLANEOUS		
L1,L2	4.7μH, 260MA, 10%	07/01/0052
L3	27μH, 260MA, 10%	07/01/032X
L4	68μH, 215MA, 10%	07/01/0168
L5	22μH, 265MA, 10%	07/01/0125
L6	12μH, 404MA, 10%	07/01/0087
LK1-LK4	Link, SKT 1MM GLD HIGHPROF 2.25 HOLE BLIND 0314 450-3366-01-03-00 FOR LK1 4 INL	
	Link, SHRTG GLD 1.02 PIN 0.25" BLUE 0314 461-2872-02-03-16	

17564 Component List (Cont.)

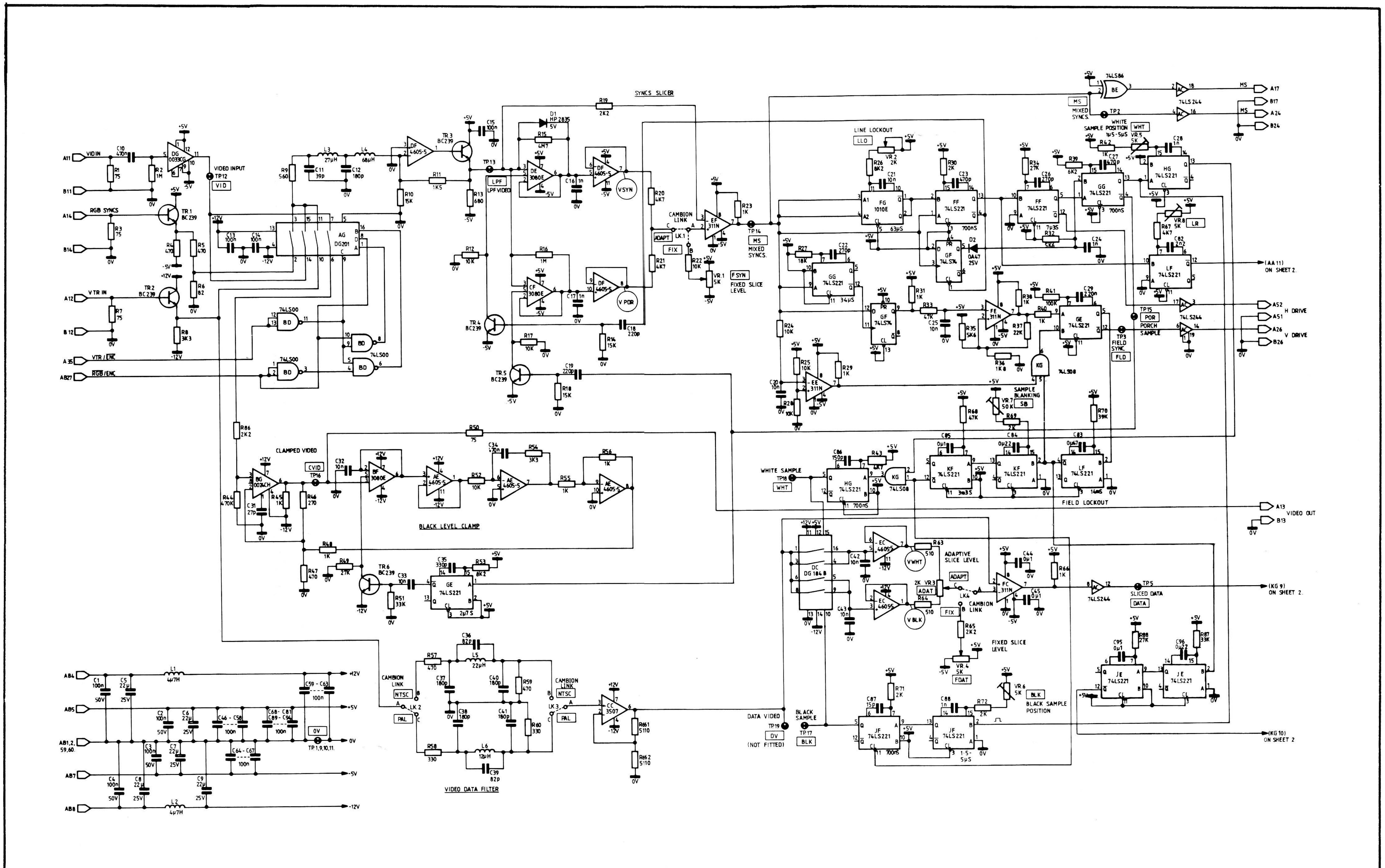


	1	2	3	4
TBC ON	OFF			
7001		ON		
7000		OFF		
FILTER COEF 0			ON	ON
FILTER COEF 1			OFF	ON
FILTER COEF 2			ON	OFF
FILTER COEF 3			OFF	OFF
STANDARD CONFIGURATION				
7000	OFF	OFF	OFF	ON
7001	OFF	ON	OFF	ON

17564, Figure 1 Input Locking Card Switch Configurations



17564, Figure 2 Input Locking Card Block Diagram



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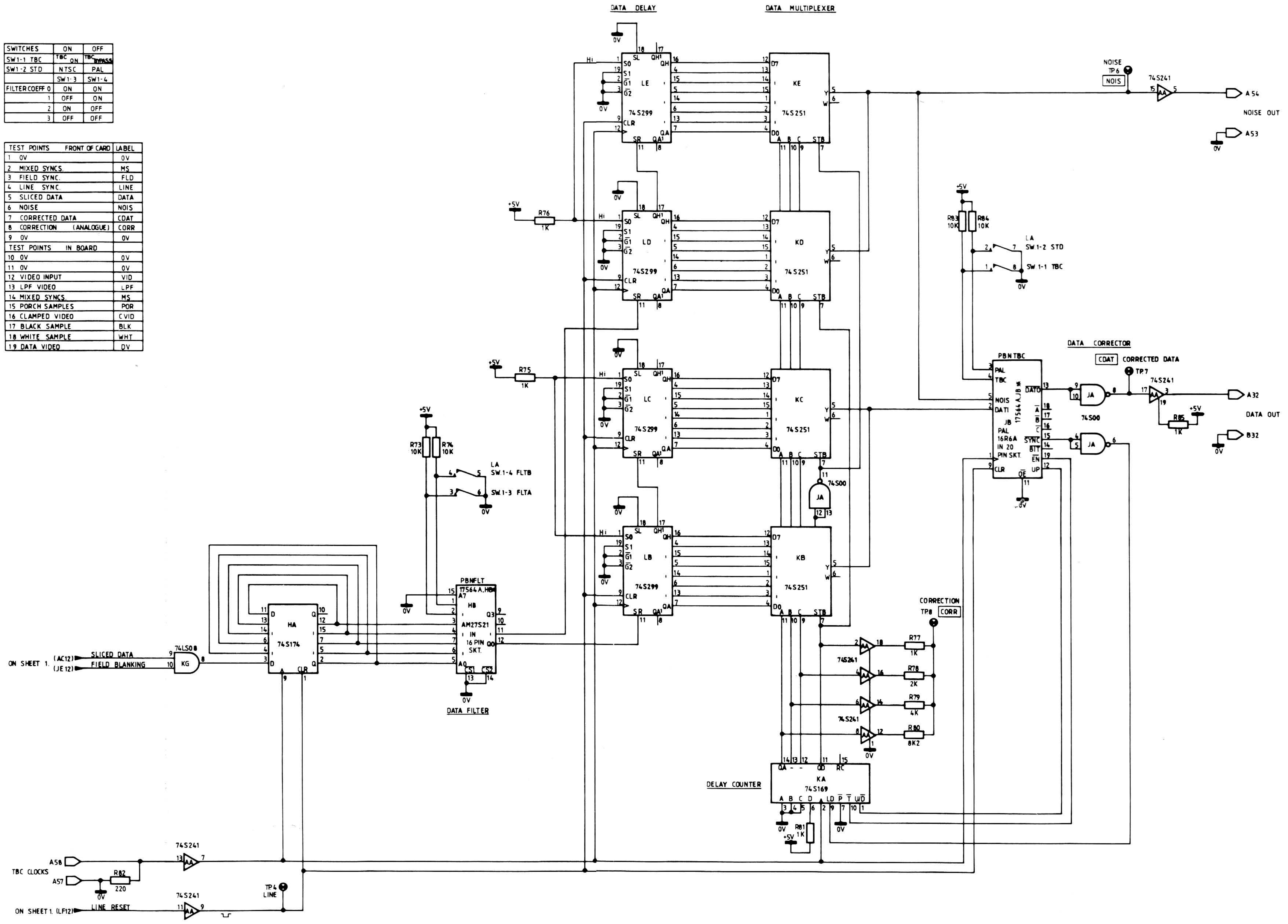
17564 Figure 3 Input Locking Card : Circuit Diagram and Component Layout
Sheet 1 of 2

SWITCHES	ON	OFF
SW1-1 TBC	TBC ON	TBC BYPASS
SW1-2 STD	NTSC	PAL
	SW1-3	SW1-4
FILTER COEFF 0	ON	ON
1	OFF	ON
2	ON	OFF
3	OFF	OFF

TEST POINTS FRONT OF CARD	LABEL
1 0V	0V
2 MIXED SYNCS.	MS
3 FIELD SYNC.	FLD
4 LINE SYNC.	LINE
5 SLICED DATA	DATA
6 NOISE	NOIS
7 CORRECTED DATA	CDAT
8 CORRECTION (ANALOGUE)	CORR
9 0V	0V
TEST POINTS IN BOARD	
10 0V	0V
11 0V	0V
12 VIDEO INPUT	VID
13 LPF VIDEO	LPF
14 MIXED SYNCS.	MS
15 PORCH SAMPLES	POR
16 CLAMPED VIDEO	CVID
17 BLACK SAMPLE	BLK
18 WHITE SAMPLE	WHT
19 DATA VIDEO	DV



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17564, Figure 3 Input Locking Card : Circuit Diagram and Component Layout

Sheet 2 of 2

5. DATA TIME BASE CORRECTOR

5.1 Introduction

This circuit corrects timing errors in the input waveform, and enables data to be recovered from video tape recorders without a time base corrector.

Input data from the adaptive slicer is re-timed to match a fixed frequency clock, which is also used to deserialise the data on the Digital Interface EBO 17480.

The circuit operates by comparing the phase of the data with an internally generated ideal and either advancing, retarding or maintaining the data in a digital delay line.

5.2 Circuit Description

The Data Time Base Corrector circuit is clocked with gated output processor picture-point clocks from the Digital Interface (A58).

NTSC	14.318MHz	6 clocks per bit
PAL	13.500MHz	4 clocks per bit

Two 16-bit serial shift registers (LB, LC and LD, LE) with 16 to 1 multiplexers on their outputs (KB, KC and KD, KE) are used to delay data and a Noise signal.

A digital filter (HA and HB) with switch adjustable coefficients detects and removes noise from the input data. Noise is defined as data with abnormal bit periods normally six clocks wide in NTSC, four in PAL. A noise signal generated for subsequent error handling in the Digital Interface and follows a parallel delay path with the data.

Filter Coefficient	Switch 1-3	Switch 1-4
0	ON	ON
1	OFF	ON
2	ON	OFF
3	OFF	OFF

The delay multiplexer is controlled by a 4-bit counter (KA) which is preset to eight at the start of each line. This allows a range of +7 to –8 clock periods of delay (approximately ±0.5µs). A simple resistor DAC on the counter output provides a test signal to monitor TBC performance. The counter is controlled by Enable and Up/Down signals.

TBC control is effected by a registered PAL (JB) which generates Enable and Up/Down counter signals and a corrected data output.

Within the PAL a 1-bit delay and logic detects positive edges in the data. The first edge after line reset sets a sync bistable (pin 15), which enables a six cycle counter for NTSC (four cycle for PAL). Switch 1-2 ON sets NTSC, OFF set PAL. The counter cycles in an ideal period, its phase being checked on subsequent data positive edges, and signals for the data delay multiplexer counter generated.

	Phase	Counter A	Counter B	Counter C	Input Data	Delay/ Enable	Counter Up/Down	Data Delay
NTSC	0	0	0	0	Late	0	0 Down	Advance
	1	1	0	0	Late	0	0 Down	Advance
	2	0	1	0	Correct	1		Same
	3	1	1	0	Early	0	1 Up	Retard
	4	0	0	1	Early	0	1 Up	Retard
	5	1	0	1		1		Same
PAL	0	0	0	0	Late	0	0 Down	Advance
	1	1	0	0	Correct	1		Same
	2	0	1	0	Early	0	1 Up	Retard
	3	1	1	0		1		Same

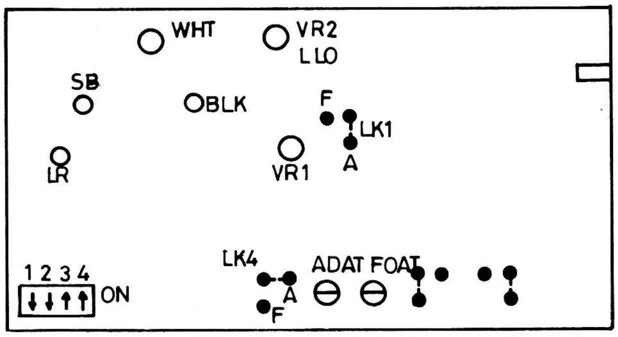
The TBC corrective action can be disabled by switch 1-1, ON.

Logic within the PAL corrects and times the data to generate a correct output with data bit periods of exactly six clocks for NTSC or four clocks for PAL.

Note that TBC clocks are only present during LOAD.

5.2.1 ADJUSTMENTS

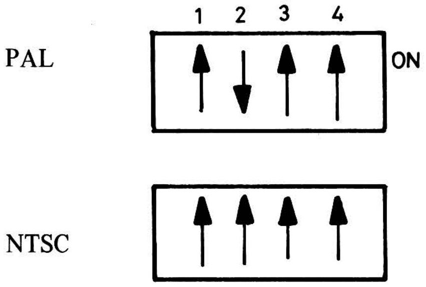
VR1	-	fixed slice level on sync slicer - selected by LK1 in F position.
VR2	-	LLO ½ line lock out - set to give one sync pulse per line during field group.
WHT BLK	-	sample positions for digital data slicer.
SB	-	sample blanking - set to black sample pulses for digital data where there are no white sync bars during field blanking.
FDAT	-	fixed slice level - selected by LK4 in F position - data slicer.
ADAT	-	modifies adaptive slice level for digital data.
LR	-	line reset pulse to Digital Interface card.



Links shown for PAL

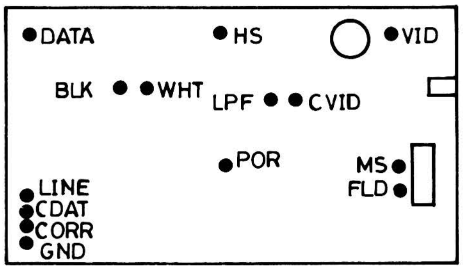
	Switch	
	ON	**OFF**
1	TBC OFF	TBC ON
2	NTSC	PAL
3	0	1 FILTER
4	0	1 COEFF.

Normal Settings



5.2.2 TEST POINTS

VID	Buffered main input video.
CVID	Clamped main input.
LPF	Filtered input - after source switch.
MS	(2 points) sliced syncs.
POR	Porch Sample
FLD	Vertical Drive.
BLK	Sample pulse for digital slicer.
WHT	Sample pulse for digital slicer.
DATA	Slice digital data before TBC.
LINE	Line reset for digital interface.
CDAT	Digital data after TBC - to Digital Interface card.
CORR	Correction signal - shows action of TBC.



1H DELAY CARD

17462

1. CIRCUIT DESCRIPTION

The VIDEO IN signal is driven from the Input Processor card and provides the 1H Delay with clamped composite video.

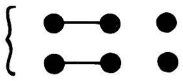
This card can be used in either of the two 1H Delay positions in the top of the rack. However, for use as the first 1H Delay a filter (L1, L2, C7, C8, C9, C10, C11, C12) is inserted in the video path, to remove any out of band signals that may be present, by use of links LK1 and LK2.

The output of the filter is buffered by voltage follower IC1 to be used as the undelayed video input to the Chroma Separator 17330; it is also passed through the Corning Delay Line DL1 and output on B16 on the 1H delayed video.

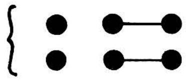
For use on the second 1H Delay card links LK1 and LK2 are used to bypass the filter and input video is passed directly to the Corning 1H Delay. The voltage follower IC1 is used as a buffer for the 1H delayed video before it is passed to the Chroma Separator.

Link positions:

Top card, delay 2



Bottom card, delay



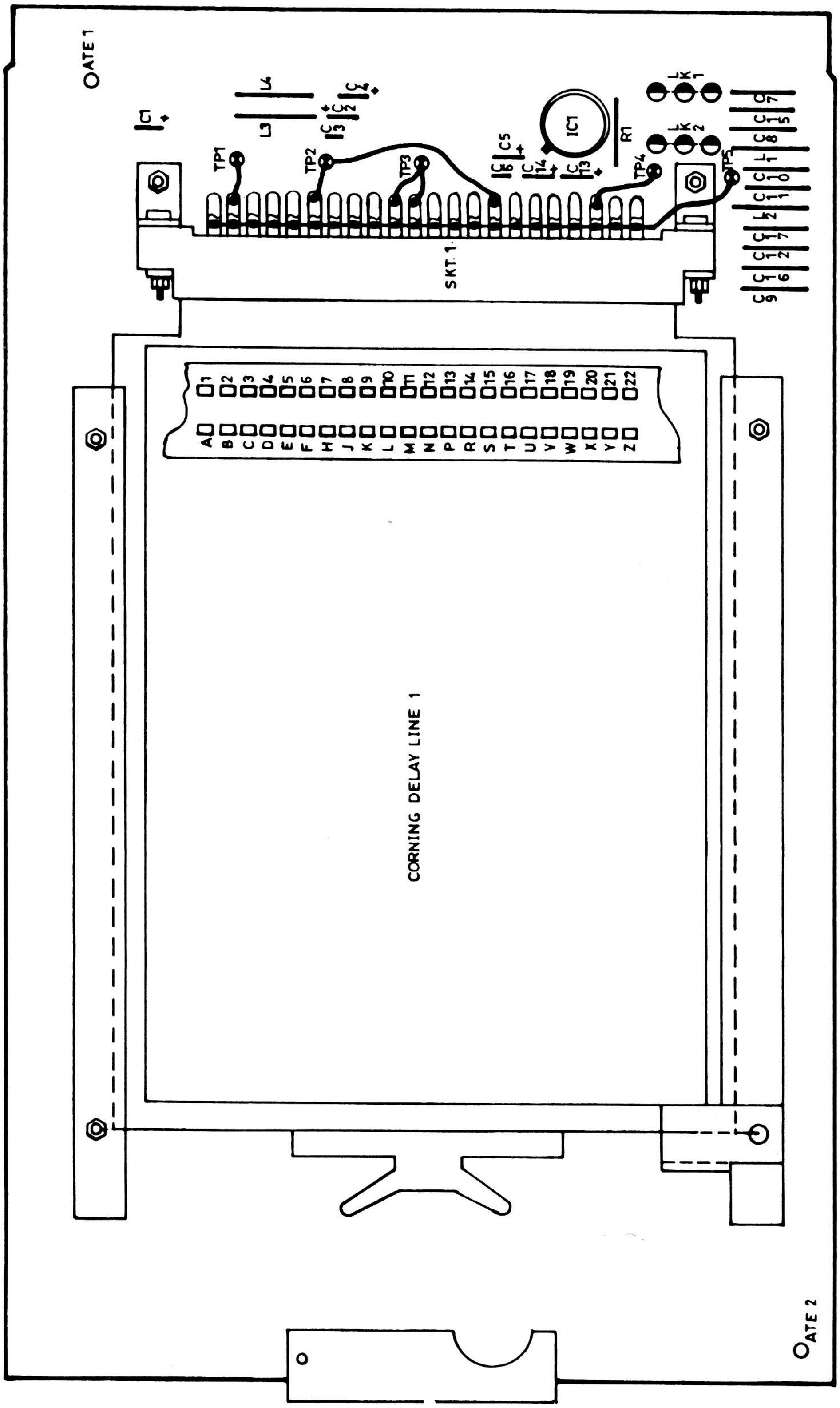
2. ADJUSTMENTS

By monitoring TP5 and TP6 on the Chroma Separator card on a dual beam oscilloscope with video input to the machine being multiburst adjust the gain and frequency response of the first delay line by use of GAIN ADJ R31 and FREQ COM ADJ C5 on the Corning Delay Line to make TP6 match TP5. (This set up should be done with correctly matched and set up oscilloscope probes.)

Adjustment of the second delay line is accomplished as above but using test points TP6 and TP12 on the Chroma Separator card.

REF.	DESCRIPTION	STOCK CODE
CAPACITORS		
C1, C2	22μF, 25V, 20%	03/03/0237
C3	100000pF, 50V, +80%-20%	03/06/0233
C4, C5	22μF, 25V, 20%	03/03/0237
C6	100000pF, 50V, +80%-20%	03/06/0233
C7	120pF, 50V, 5%	03/04/0232
C8	68pF, 50V, 5%	03/04/0208
C9	330pF, 50V, 5%	03/04/0348
C10	33pF, 50V, 5%	03/04/016X
C11	22pF, 50V, 5%	03/04/0135
C12	220pF, 50V, 5%	03/04/0305
C13, C14	6.8μF, 25V, 20%	03/03/0148
C15	47pF, 50V, 5%	03/04/0186
C16	22pF, 50V, 5%	03/04/0135
C17	10pF, 50V, 0.5%	03/04/0097
RESISTORS		
R1	75Ω, 250mW, 2%, 100ppm	01/01/0263
INTEGRATED CIRCUITS		
IC1	0033CG	04/02/0111
MISCELLANEOUS		
L1	Inductor 10μH, 830mA, 10%	07/01/0028
L2	Inductor 10.5μH, 600mA, 10%	07/01/0281
L3, L4	Inductors 40.7μH, 260mA, 10%	07/01/0052
SK1	Socket 22W	08/03/0146

17462 Component List


ATE 1
ATE 2
C1
L3
L4
C2
C3
C4
TP1
TP2
TP3
TP4
TP5
C5
C6
C14
C13
IC1
R1
LK1
LK2
C7
C15
C18
L1
C10
C11
L2
C17
C12
C16
C9
SKT. 1.
17462
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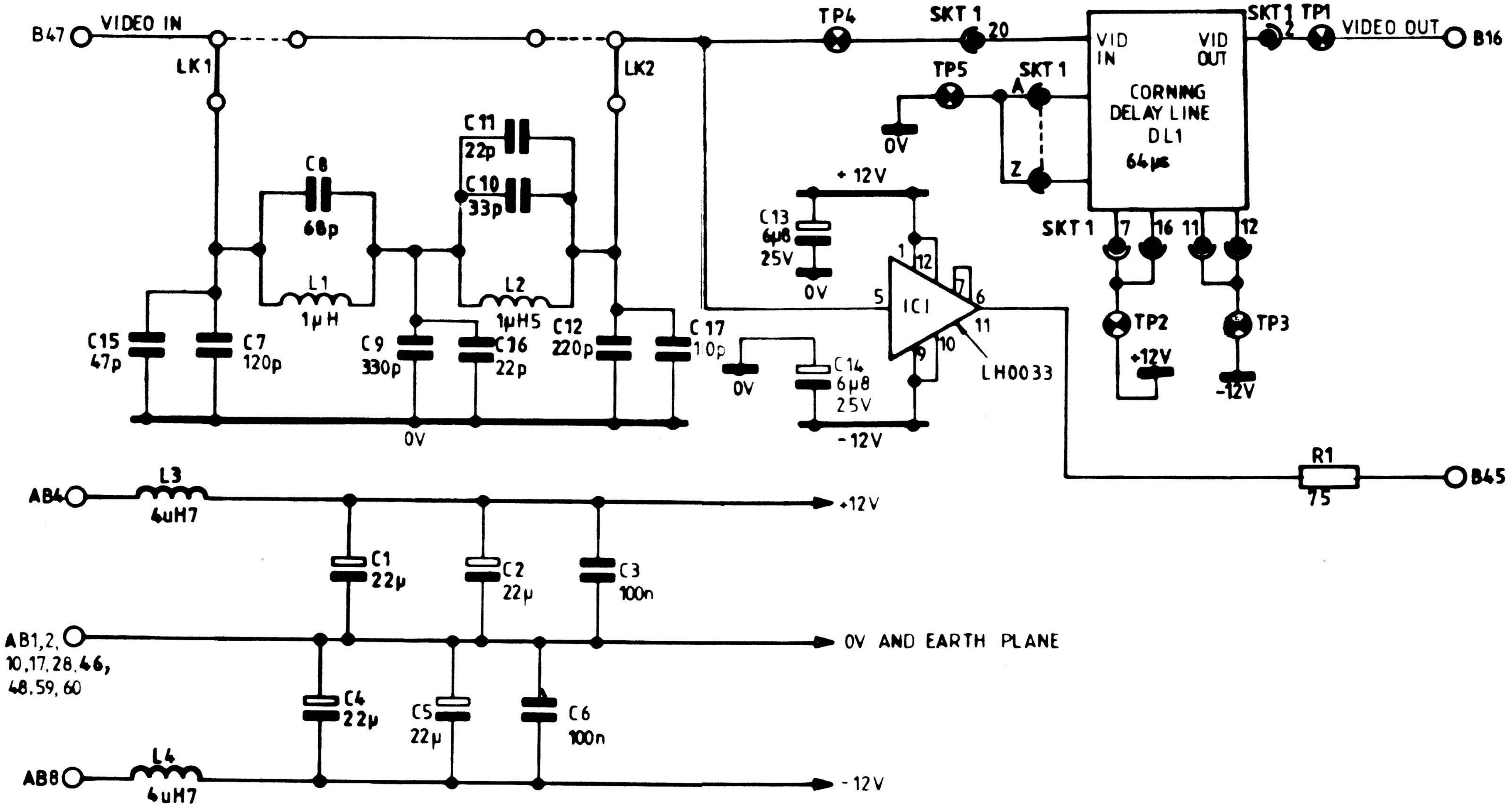
U
V
W
X
Y
Z
CORNING DELAY LINE 1



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17462, Figure 1 1H Delay Card : Circuit Diagram and Component Layout

ADC CARD

17402

1. INTRODUCTION

The ADC card accepts either Y, U, V video signals from the Chroma Separator card or R, G, B video signals from an external source and converts the selected video inputs into two streams of 8-bit digital data.

2. CIRCUIT DESCRIPTION

The data outputs represent Luminance (Y) and Chrominance (U/V). Luminance signals from a 5.5MHz bandwidth are converted at a 13.5MHz (14.31MHz for NTSC) sampling rate. The U and V components each have a bandwith of 2.5MHz and are sampled at 6.75MHz, (7.15MHz for NTSC), by a common ADC.

3. SIGNAL INPUT

The RGB signal inputs are buffered by three identical amplifiers. Taking the red input as an example; the video input is a.c. coupled to the base of TR1, R1 acting as the 75Ω line terminating resistor. TR1, TR2 produce an output voltage swing at the emitter of TR2 which is forwarded to the colour encoding resistor matrix. Current from TR44 via D2 saturates the base of TR2 effectively inhibiting amplifier output when Y, U, V inputs are selected and the R, G, B inputs are not required.

The input colour encoding matrix provides information to each of three multipliers, (IC, IB, IA), which produce the required Y, U, and V encoded outputs. The relationship of each colour input and resistors to multiplier inputs are given in Table 1.

INPUTS	Y OUTPUT MULTIPLIER (IC)	U OUTPUT MULTIPLIER (IB)	V OUTPUT MULTIPLIER (IA)
R	R6 and R9 (+)	R7 and R10 (–)	R8 (+)
B	R77 and R80 (+)	R78 (–)	R79 (–)
G	R122 and R125 (+)	R123 (+)	R124, R127, and R131 (–)

Note: (+) indicates connection to non inverting input.
(–) connection to inverting input.

17402, Table 1 ADC Card : Relationship Between Colour Inputs and Resistors to Multiplier Inputs

The luminance signal (Y) is produced by the addition of colour components, the colour difference signals (U and V) by the subtraction of colour pairs. The gain of each multiplier is set by VR1, VR2 and VR3 accessible from the front of the card. TR48, TR49 and TR50 act as current sources for the three multipliers, and when these current sources are switched off, the multipliers become inactive. The outputs of the three multipliers are parallel connected to the outputs of the three multipliers HC, HB, HA which process the Y, U, V inputs to this card.

The Y, U and V inputs are applied directly to the inputs of multipliers HC, HB and HA respectively. Overall gain for the multipliers is buffered at FC8 from the front panel control and chroma gain is input directly to HB8 and HA8. TR45 and TR46 act as current sources for these three multipliers and when these sources are switched off during RGB input, the multipliers become inactive.

The current sources TR44 to TR50 inclusive are controlled by the logic input ENC/RGB inverter ID (pins 6 and 4) providing current sinks for inhibited current sources.

4. Y, U AND V SIGNAL PROCESSING

The Y, U and V signal streams are each processed in a similar fashion, the Y processing is described in this paragraph as an example, differences in the U and V processing are detailed as necessary. The current swing output by multiplier HC pins 2 and 14 is converted into a voltage swing by the transimpedance amplifier made up of TR3, TR5, TR4 and TR6. TR3 and TR5 detect differential current and produce a voltage output at the collector of TR5. TR4 and TR6 are configured as a current mirror to drive the base of TR8.

A virtual earth mixing amplifier is used to regulate input voltage swings and present the ADC with a constant range of voltages at its sample input. The virtual earth mixing point has three sources imposed upon it, the input signal from TR5, TR6, negative feedback from the amplifier output via R44 and an integrated black level clamping signal supplied via R48. The generation of this signal is described later.

The mixing amplifier comprises TR8 which controls the gain, TR9 which is an impedance buffer and

TR10 which acts as a current source to ensure a symmetrical output into R50. A Mathey filter provides low pass filtering for the signal to limit the maximum frequency presented to the ADC to 5.5MHz.

The Y signal passes from the filter output through buffer CC to the ADC BB. The U and V signal chains are multiplexed to buffer DA and ADC BA by the MPX CLOCK signal which controls the switching network made up of TR26, TR27 and diodes D12 to D15 inclusive.

Each signal chain uses an identical feedback clamp, the Y signal chain is again used as an example.

The analogue input of the ADC is input to the sample and hold amplifier EC via R58. The sample command for this amplifier is developed from the SYNC signal by monostable AG which switches on TR14 for a set period after the SYNC signal is first detected. In the selected period after a sync pulse, video should be at black level therefore pin 2 of EC holds a black level sample for each received line. This sample is buffered through FC5 and mixed with BLACK LEVEL at FC2; BLACK LEVEL is set by a front panel control. The difference signal output at FC1 is integrated at FC14 and imposed on the virtual earth mixing point via R48 thus completing the closed loop control for the video input. For the U and V signal chains MPX CLOCK in conjunction with SYNC and monostables BC and DC switch alternate sample voltages to the U sample and hold amplifier FB5 and the V sample and hold amplifier FA5.

5. CONVERSION TO DATA

ADCs BB and BA using stable voltage reference sources sample the analogue input at 13.5MHz (14.31MHz for NTSC) and output a stream of 8-bit data. Buffers AD, AC, AB and AA convert the data to ECL complementary logic output to reduce transmitted noise within the equipment card cage.

REF.	DESCRIPTION	STOCK CODE
CAPACITORS		
C1	470000pF, 63V, 10%	03/05/0262
C2-C4	10000pF, 100V, +80% –20%	03/06/0101
C5,C6	NOT FITTED	
C7	10000pF, 100V, +80% –20%	03/06/0101
C8,C9	NOT FITTED	
C10	10000pF, 100V, +80% –20%	03/06/0101
C11	82pF, 100V, 20%	03/06/0624
C12	100000pF, 50V, +80% –20%	03/06/0233
C13,C14	NOT FITTED	
C15-C17	100000pF, 50V, +80% –20%	03/06/0233
C18	33pF, 100V, 10%	03/06/0489
C19	100000pF, 50V, +80% –20%	03/06/0233
C20	22μF, 16V, 20%	03/03/0253
C21	10000pF, 100V, +80% –20%	03/06/0101
C22	22μF, 16V, 20%	03/03/0253
C23	220pF, 100V, 10%	03/06/0055
C24	1μF, 35V, 20%	03/03/004Y
C25-C28	100000pF, 50V, +80% –20%	03/06/0233
C29	68000pF, 63V, 10%	03/05/0378
C30	15000pF, 100V, +80% –20%	03/06/011X
C31,C32	10000pF, 100V, +80% –20%	03/06/0101
C33	470000pF, 63V, 10%	03/05/0262
C34-C39	10000pF, 100V, +80% –20%	03/06/0101
C40,C41	NOT FITTED	
C42-C44	100000pF, 50V, +80% –20%	03/06/0233
C45-C47	NOT FITTED	
C48,C49	100000pF, 50V, +80% –20%	03/06/0233
C50	NOT FITTED	
C51	22μF, 16V, 20%	03/03/0253
C52	1μF, 35V, 20%	03/03/004Y
C53-C56	100000pF, 50V, +80% –20%	03/06/0233
C58-C65	10000pF, 100V, +80% –20%	03/06/0101
C66,C67	100000pF, 50V, +80% –20%	03/06/0233
C68-C71	2.2μF, 16V, 20%	03/03/0067
C72,C73	100000pF, 50V, +80% –20%	03/06/0233
C74	33pF, 100V, 10%	03/06/0489
C75,C76	100000pF, 50V, +80% –20%	03/06/0233
C77-C81	1000pF, 100V, 10%	03/06/0314
C82	680pF, 100V, 10%	03/06/0063
C83	10000pF, 100V, +80% –20%	03/06/0101
C84	NOT FITTED	
C85-C88	47μF, 16V, 20%	03/03/027X
C89-C101	100000pF, 50V, +80% –20%	03/06/0233
C102	NOT FITTED	
C103-C110	100000pF, 50V, +80% –20%	03/06/0233
C111	6.8μF, 16V, 20%	03/03/013X
C112	100000pF, 50V, +80% –20%	03/06/0233
C113	1μF, 35V, 20%	03/03/004Y
C114	470000pF, 63V, 10%	03/05/0262
C115	NOT FITTED	
C116	1μF, 35V, 20%	03/03/004Y
C117	2.2μF, 25V, 20%	03/03/0318
C118	22μF, 16V, 20%	03/03/0253
CAPACITORS (Cont)		
C119	8.2pF, 63V, OP25	03/00/0206
VC1,VC2	3.5-25pF, 50V	03/07/0212
RESISTORS		
R1	75Ω, 250mW, 2%, 100ppm	01/01/0263
R2	470kΩ, 250mW, 2%, 100ppm	01/01/179Y
R3	100kΩ, 250mW, 2%, 100ppm	01/01/1162
R4	1kΩ, 250mW, 2%, 100ppm	01/01/0646
R5	100Ω, 250mW, 2%, 100ppm	01/01/0336
R6	1.4kΩ, 250mW, 2%, 100ppm	01/01/165Y
R7	2.7kΩ, 250mW, 2%, 100ppm	01/01/0743
R8	1kΩ, 250mW, 2%, 100ppm	01/01/0646
R9,R10	270Ω, 250mW, 2%, 100ppm	01/01/0476
R11	NOT FITTED	
R12	4.99kΩ, 250mW, 1%, 50ppm	01/01/0859
R13	NOT FITTED	
R14	47kΩ, 250mW, 2%,	01/01/1103
R15	1.8kΩ, 250mW, 2%, 100ppm	01/01/070Y
R16	1kΩ, 250mW, 2%, 100ppm	01/01/0646
R17	2kΩ, 250mW, 2%, 100ppm	01/01/0719
R18	4.7kΩ, 250mW, 2%, 100ppm	01/01/084Y
R20	NOT FITTED	
R21	12kΩ, 250mW, 2%,	01/01/0964
R22	NOT FITTED	
R23	12kΩ, 250mW, 2%, 100ppm	01/01/0964
R24	1kΩ, 250mW, 2%, 100ppm	01/01/0646
R25-R27	NOT FITTED	
R28	75Ω, 250mW, 2%, 100ppm	01/01/0263
R29	1kΩ, 250mW, 2%, 100ppm	01/01/0646
R30	1.8kΩ, 250mW, 2%, 100ppm	01/01/070Y
R31,R32	47kΩ, 250mW,2%, 100ppm	01/01/1103
R34	1kΩ, 250mW, 2%, 100ppm	01/01/0646
R35	4.7kΩ, 250mW, 2%, 100ppm	01/01/084Y
R36	330Ω, 250mW, 2%, 100ppm	01/01/1723
R37	1kΩ, 250mW, 2%, 100ppm	01/01/0646
R38	330Ω, 250mW, 2%, 100ppm	01/01/1723
R39	1kΩ, 250mW, 2%, 100ppm	01/01/0646
R40	NOT FITTED	
R41	47kΩ, 250mW, 2%, 100ppm	01/01/1103
R42	1.8kΩ, 250mW, 2%, 100ppm	01/01/070Y
R43	1.5kΩ, 250mW, 2%, 100ppm	01/01/0697
R44	8.2kΩ, 250mW, 2%, 100ppm	01/01/0921

17402 Component List

RESISTORS (Cont)

REF.	DESCRIPTION	STOCK CODE
C45	4.7kΩ, 250mW, 2%, 100ppm	01/01/084Y
R46	1.8kΩ, 250mW, 2%, 100ppm	01/01/070Y
R47	47Ω, 250mW, 2%, 100ppm	01/01/0204
R48	2.2kΩ, 250mW, 2%, 100ppm	01/01/1642
R49	NOT FITTED	
R50	75Ω, 250mW, 2%, 100ppm	01/01/0263
R51	560Ω, 250mW, 2%, 100ppm	01/01/0581
R52	75Ω, 250mW, 2%, 100ppm	01/01/0263
R53	1kΩ, 250mW, 2%, 100ppm	01/01/0646
R54	33kΩ, 250mW, 2%, 100ppm	01/01/1065
R55	1kΩ, 250mW, 2%, 100ppm	01/01/0646
R56	NOT FITTED	
R57	10Ω, 250mW, 2%, 100ppm	01/01/005Y
R58	1kΩ, 250mW, 2%, 100ppm	01/01/0646
R59	15kΩ, 250mW, 2%, 100ppm	01/01/0972
R60	NOT FITTED	
R61	24kΩ, 250mW, 2%, 100ppm	01/01/1022
R62	1.5kΩ, 250mW, 2%, 100ppm	01/01/0697
R63	3.9kΩ, 250mW, 2%, 100ppm	01/01/0808
R64	1kΩ, 250mW, 2%, 100ppm	01/01/0646
R65	100Ω, 250mW, 2%, 100ppm	01/01/0336
R66	470Ω, 250mW, 2%, 100ppm	01/01/0557
R67	330Ω, 250mW, 2%, 100ppm	01/01/1723
R68	10kΩ, 250mW, 2%, 100ppm	01/01/0948
R69	12kΩ, 250mW, 2%, 100ppm	01/01/0964
R70	3.3kΩ, 250mW, 2%, 100ppm	01/01/0786
R71	150kΩ, 250mW, 2%, 100ppm	01/01/1669
R72	75Ω, 250mW, 2%, 100ppm	01/01/0263
R73	470kΩ, 250mW, 2%, 100ppm	01/01/179Y
R74	100kΩ, 250mW, 2%, 100ppm	01/01/1162
R75	100Ω, 250mW, 2%, 100ppm	01/01/0336
R76	1kΩ, 250mW, 2%, 100ppm	01/01/0646
R77	100Ω, 250mW, 2%, 100ppm	01/01/0336
R78	1.5kΩ, 250mW, 2%, 100ppm	01/01/0697
R79	1.2kΩ, 250mW, 2%, 100ppm	01/01/0662
R80	750Ω, 250mW, 2%, 100ppm	01/01/0603
R81,R82	NOT FITTED	
R83	4.99kΩ, 250mW, 1%, 50ppm	01/01/0859
R84,R85	NOT FITTED	
R86	1.8kΩ, 250mW, 2%, 100ppm	01/01/070Y

RESISTORS (Cont)

REF.	DESCRIPTION	STOCK CODE
R87,R88	1kΩ, 250mW, 2%, 100ppm	01/01/0646
R89	4.7kΩ, 250mW, 2%, 100ppm	01/01/084Y
R90,R91	NOT FITTED	
R92	75Ω, 250mW, 2%, 100ppm	01/01/0263
R93	1kΩ, 250mW, 2%, 100ppm	01/01/0646
R94	1.8kΩ, 250mW, 2%, 100ppm	01/01/070Y
R95	1.1kΩ, 250mW, 2%, 100ppm	01/01/0654
R96	2kΩ, 250mW, 2%, 100ppm	01/01/0719
R97	4.7kΩ, 250mW, 2%, 100ppm	01/01/084Y
R98,R99	330Ω, 250mW, 2%, 100ppm	01/01/1723
R100,R101	1kΩ, 250mW, 2%, 100ppm	01/01/0646
R102	1.8kΩ, 250mW, 2%, 100ppm	01/01/070Y
R103	100Ω, 250mW, 2%, 100ppm	01/01/0336
R104	1.5kΩ, 250mW, 2%, 100ppm	01/01/0697
R105	4.7kΩ, 250mW, 2%, 100ppm	01/01/084Y
R106	1.8kΩ, 250mW, 2%, 100ppm	01/01/070Y
R107	68Ω, 250mW, 2%, 100ppm	01/01/0247
R108	4.7kΩ, 250mW, 2%, 100ppm	01/01/084Y
R109,R110	75Ω, 250mW, 2%, 100ppm	01/01/0263
R111	1kΩ, 250mW, 2%, 100ppm	01/01/0646
R112	3.9kΩ, 250mW, 2%, 100ppm	01/01/0808
R113	1.5kΩ, 250mW, 2%, 100ppm	01/01/0697
R114	100Ω, 250mW, 2%, 100ppm	01/01/0336
R115	470Ω, 250mW, 2%, 100ppm	01/01/0557
R116	330Ω, 250mW, 2%, 100ppm	01/01/1723
R117	75Ω, 250mW, 2%, 100ppm	01/01/0263
R118	470kΩ, 250mW, 2%, 100ppm	01/01/179Y
R119	100kΩ, 250mW, 2%, 100ppm	01/01/1162
R120	100Ω, 250mW, 2%, 100ppm	01/01/0336
R121	1kΩ, 250mW, 2%, 100ppm	01/01/0646
R122	3.9kΩ, 250mW, 2%, 100ppm	01/01/0808
R123	1kΩ, 250mW, 2%, 100ppm	01/01/0646
R124	3.9kΩ, 250mW, 2%, 100ppm	01/01/0808
R125	1.4kΩ, 250mW, 2%, 100ppm	01/01/165Y
R126	NOT FITTED	
R127	2.2kΩ, 250mW, 2%, 100ppm	01/01/1642
R128	4.99kΩ, 250mW, 1%, 100ppm	01/01/0859
R129	NOT FITTED	
R130	1.8kΩ, 250mW, 2%, 100ppm	01/01/070Y

17402 Component List (Cont)

RESISTORS (Cont)

REF.	DESCRIPTION	STOCK CODE
R131	10kΩ, 250mW, 2%, 100ppm	01/01/0948
R132,R133	1kΩ, 250mW, 2%, 100ppm	01/01/0646
R134	4.7kΩ, 250mW, 2%, 100ppm	01/01/084Y
R135,R136	NOT FITTED	
R137	10kΩ, 250mW, 2%, 100ppm	01/01/0948
R138	2kΩ, 250mW, 2%, 100ppm	01/01/0719
R139	75Ω, 250mW, 2%, 100ppm	01/01/0263
R140	1kΩ, 250mW, 2%, 100ppm	01/01/0646
R141	1.8kΩ, 250mW, 2%, 100ppm	01/01/070Y
R142	1.1kΩ, 250mW, 2%, 100ppm	01/01/0654
R143	2kΩ, 250mW, 2%, 100ppm	01/01/0719
R144	330Ω, 250mW, 2%, 100ppm	01/01/1723
R145	1kΩ, 250mW, 2%, 100ppm	01/01/0646
R146	4.7kΩ, 250mW, 2%, 100ppm	01/01/084Y
R147	330Ω, 250mW, 2%, 100ppm	01/01/1723
R148	1kΩ, 250mW, 2%, 100ppm	01/01/0646
R149	1.8kΩ, 250mW, 2%, 100ppm	01/01/070Y
R150	4.7kΩ, 250mW, 2%, 100ppm	01/01/084Y
R151	1.5kΩ, 250mW, 2%, 100ppm	01/01/0697
R152,R153	4.7kΩ, 250mW, 2%, 100ppm	01/01/084Y
R154	1kΩ, 250mW, 2%, 100ppm	01/01/0646
R155	68Ω, 250mW, 2%, 100ppm	01/01/0247
R156	1MΩ, 330mW, 5%, 50ppm	01/01/1332
R157	4.7kΩ, 250mW, 2%, 100ppm	01/01/084Y
R158	75Ω, 250mW, 2%, 100ppm	01/01/0263
R159-R166	NOT FITTED	
R167	1MΩ, 330mW, 5%, 250ppm	01/01/1332
R168,R169	560Ω, 250mW, 2%, 100ppm	01/01/0581
R170	75Ω, 250mW, 2%, 100ppm	01/01/0263
R171,R172	33kΩ, 250mW, 2%, 100ppm	01/01/1065
R173,R174	15kΩ, 250mW, 2%, 100ppm	01/01/0972
R175,R176	3.9kΩ, 250mW, 2%, 100ppm	01/01/0808
R177	100Ω, 250mW, 2%, 100ppm	01/01/0336
R178	NOT FITTED	
R179	4.3kΩ, 250mW, 2%, 100ppm	01/01/0832
R180	15kΩ, 250mW, 2%, 100ppm	01/01/0972
R181-R183	NOT FITTED	
R184	10Ω, 250mW, 2%, 100ppm	01/01/005Y
R185	1kΩ, 250mW, 2%, 100ppm	01/01/0646
R186-R189	1kΩ x 8, 125mW, 5%, 300ppm	01/08/0539

RESISTORS (Cont)

REF.	DESCRIPTION	STOCK CODE
R190	4.7kΩ, 250mW, 2%, 100ppm	01/08/102Y
R191	2.2kΩ, 250mW, 2%, 100ppm	01/01/1642
R192,R193	100Ω, 250mW, 2%, 100ppm	01/01/0336
R194	560Ω, 250mW, 2%, 100ppm	01/01/0581
R195	3.6kΩ, 250mW, 2%, 100ppm	01/01/0794
R196	910Ω, 250mW, 2%, 100ppm	01/01/062X
R197	NOT FITTED	
R198	100Ω, 250mW, 2%, 100ppm	01/01/0336
R199	470Ω, 250mW, 2%, 100ppm	01/01/0557
R200	1kΩ, 250mW, 2%, 100ppm	01/01/0646
R201	560Ω, 250mW, 2%, 100ppm	01/01/0581
R202	470Ω, 250mW, 2%, 100ppm	01/01/0557
R203	100Ω, 250mW, 2%, 100ppm	01/01/0336
R204	1kΩ, 250mW, 2%, 100ppm	01/01/0646
R205	100Ω, 250mW, 2%, 100ppm	01/01/0336
R206	750Ω, 250mW, 2%, 100ppm	01/01/0603
R207	390Ω, 250mW, 2%, 100ppm	01/01/053Y
R209	100Ω, 250mW, 2%, 100ppm	01/01/0336
R210	10kΩ, 250mW, 2%, 100ppm	01/01/0948
R211	NOT FITTED	
R212	100Ω, 250mW, 2%, 100ppm	01/01/0336
R213,214	100kΩ, 250mW, 2%, 100ppm	01/01/1162
R215	47kΩ, 250mW, 2%, 100ppm	01/01/1103
R216	1kΩ, 250mW, 2%, 100ppm	01/01/0646
VR1-VR3	1kΩ, 1W, 10%	02/01/007Y
VR4	NOT FITTED	
VR5	2kΩ, 500mW, 10%	02/02/005X
VR6	10kΩ, 500mW, 10%	02/02/0076
VR7	50kΩ, 500mW, 10%	02/04/0093

SEMICONDUCTORS

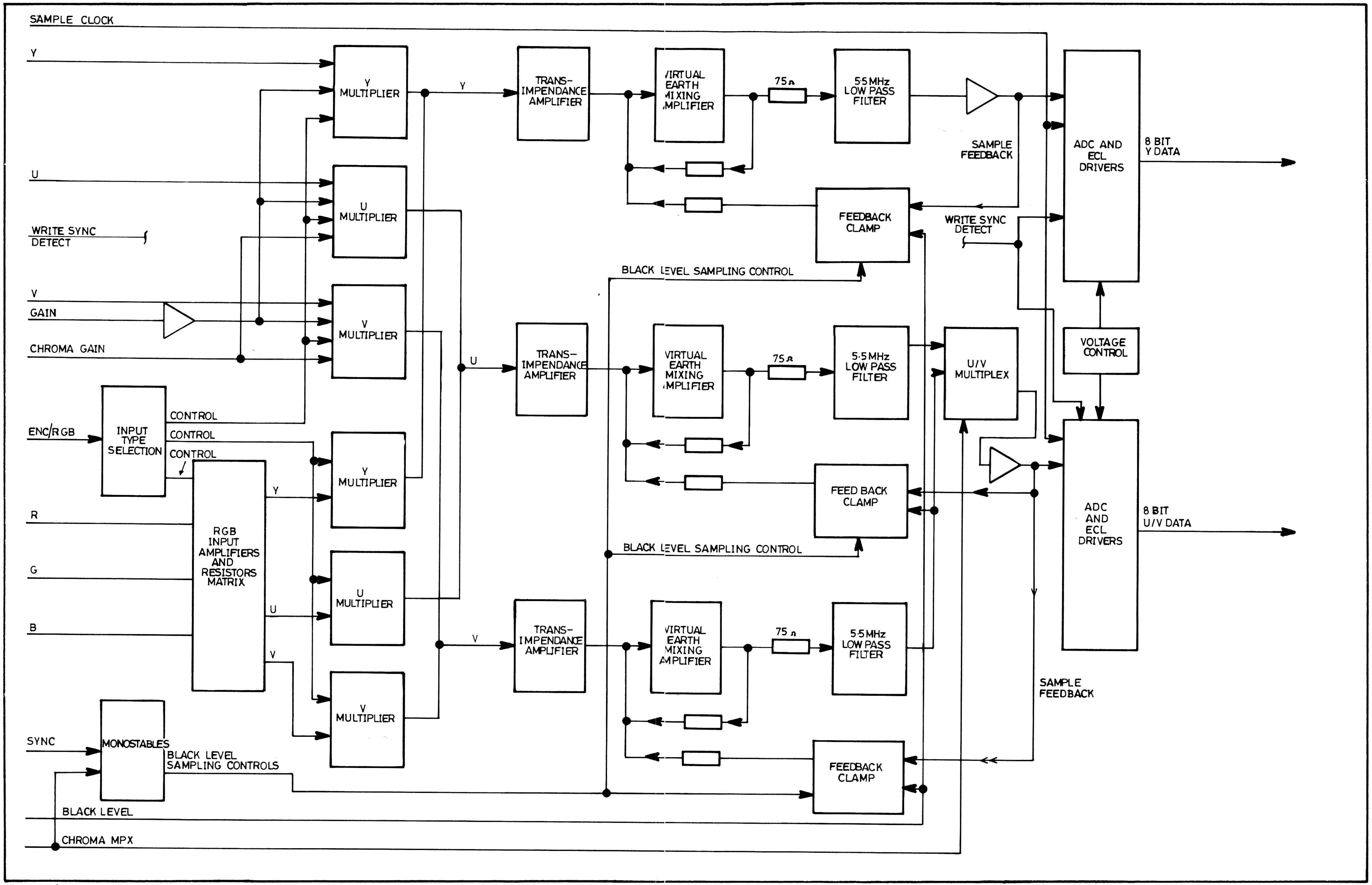
REF.	DESCRIPTION	STOCK CODE
D1-D11	IN916, 75V, 500M	06/01/0083
D12-D15	TA 50822835, 5V	06/01/0075
ZD1	TA IN827A,	06/02/0062
ZD2,ZD3	TA BZY88C, 5.6V, 500mW	06/02/0208
ZD4	IN827A, 6.2V, 400mW	06/02/0062
ZD5	TA BZT88C, 5.6V, 500mW	06/02/0208
TR1,TR2	NPN NC239C, 45V	05/01/0446
TR3	PNP BC309C, 45V	05/01/0454
TR4	NPN BC239C, 45V	05/01/0446
TR5	PNP BC309C, 45V	05/01/0454
TR6	NPN BC239C, 45V	05/01/0446
TR7	NPN 2N918, 30V	05/01/002Y
TR8	NPN BC239C, 45V,	05/01/0446
TR9,TR10	NPN 2N2219, 60V	05/01/0039
TR11	PNP BC309C, 45V	05/01/0454
TR12	NPN 2N2219, 60V	05/01/0039
TR13-TR18	NPN BC239C, 45V	05/01/0446
TR19,TR20	PNP BC309C	05/01/0454
TR21	NPN BC239C, 45V	05/01/0446

17402 Component List (Cont)

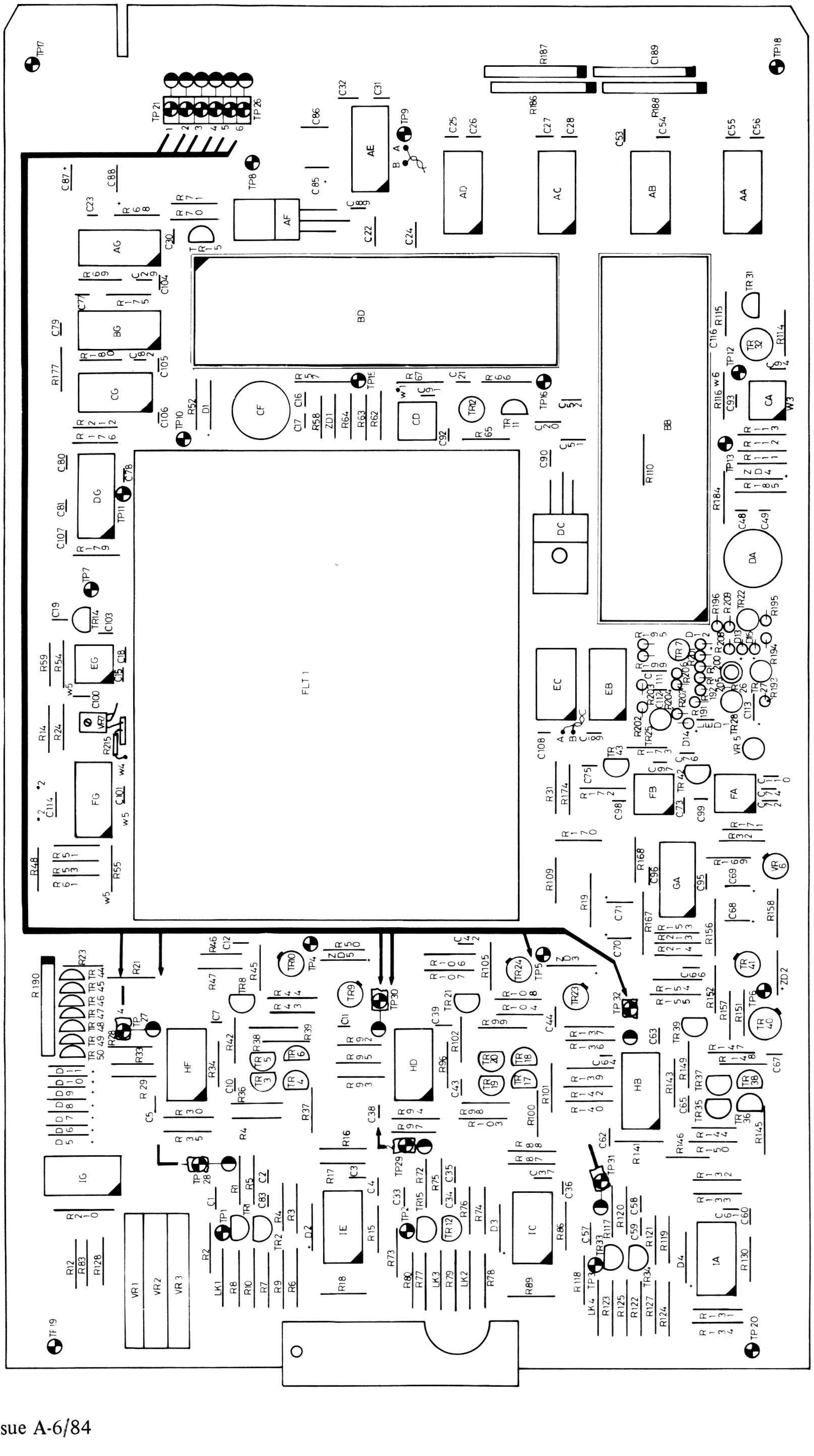
REF.	DESCRIPTION	STOCK CODE
SEMICONDUCTORS (Cont)		
TR22	NPN 2N918, 30V	05/01/002Y
TR23,TR24	NPN 2N2219, 60V	05/01/0039
TR25-TR28	NPN 2N918, 30V	05/01/002Y
TR29,TR30	NOT FITTED	
TR31	PNP BC309C, 45V	05/01/0454
TR32	NPN 2N2219, 60V	05/01/0039
TR33,TR34	NPN BC239C, 45V	05/01/0446
TR35	PNP BC309C, 45V	05/01/0454
TR36	NPN BC239C, 45V	05/01/0446
TR37	PNP BC309C, 45V	05/01/0454
TR38,TR39	NPN BC239C, 45V	05/01/0446
TR40,TR41	NPN 2N2219, 60V	05/01/0039
TR42,TR43	NPN BC239C, 45V	05/01/0446
TR44-TR50	PNP ZTX212AL, 60V	05/01/0276
INTEGRATED CIRCUITS		
AA-AD	ECL 10124P	04/01/207Y
AE	ECL 10125P	04/01/2089
AF	LIN 7906UC, 6V	05/04/0086
BB-BD	TTL 1107J	04/01/5363

REF.	DESCRIPTION	STOCK CODE
INTEGRATED CIRCUITS (Cont)		
BG	74LS221N	04/01/1589
CA-CC	LIN 741CN	04/01/250X
CF	LIN 0033CG	04/02/0111
CG	74S86N	04/01/0825
DA	LIN 0033CG	04/02/0111
DC	7906UC	05/04/0086
DG	74LS221N	04/01/1589
EB	74S86N	04/01/0825
EC	74S00N	04/01/0035
EG	LIN 3080E	04/03/3043
FA,FB	LIN 3080E	04/03/3043
FG-GA	LIN 4605-5	04/03/1598
HB-IE	LIN 1495L	04/01/1902
IG	74LS05N	04/01/4758
MISCELLANEOUS		
LK1-LK4	Link	31/02/0069
FLT1	Filter	30/02/017Y

17402 Component List (Cont)



17402, Figure 1 ADC Card Block Diagram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TP18
TP19
TP20
17402
TP21
TP26
TP8
TP9
AE
AF
AD
AC
AB
AA
BD
BB
CF
CD
CA
DC
DA
AG
BG
CG
DG
EG
FG
FLT1
EC
EB
FB
FA
GA
HF
HD
HB
IG
IE
IC
IA
VR1
VR2
VR3
R187
R186
C189
R188
R190
TP10
TP11
TP12
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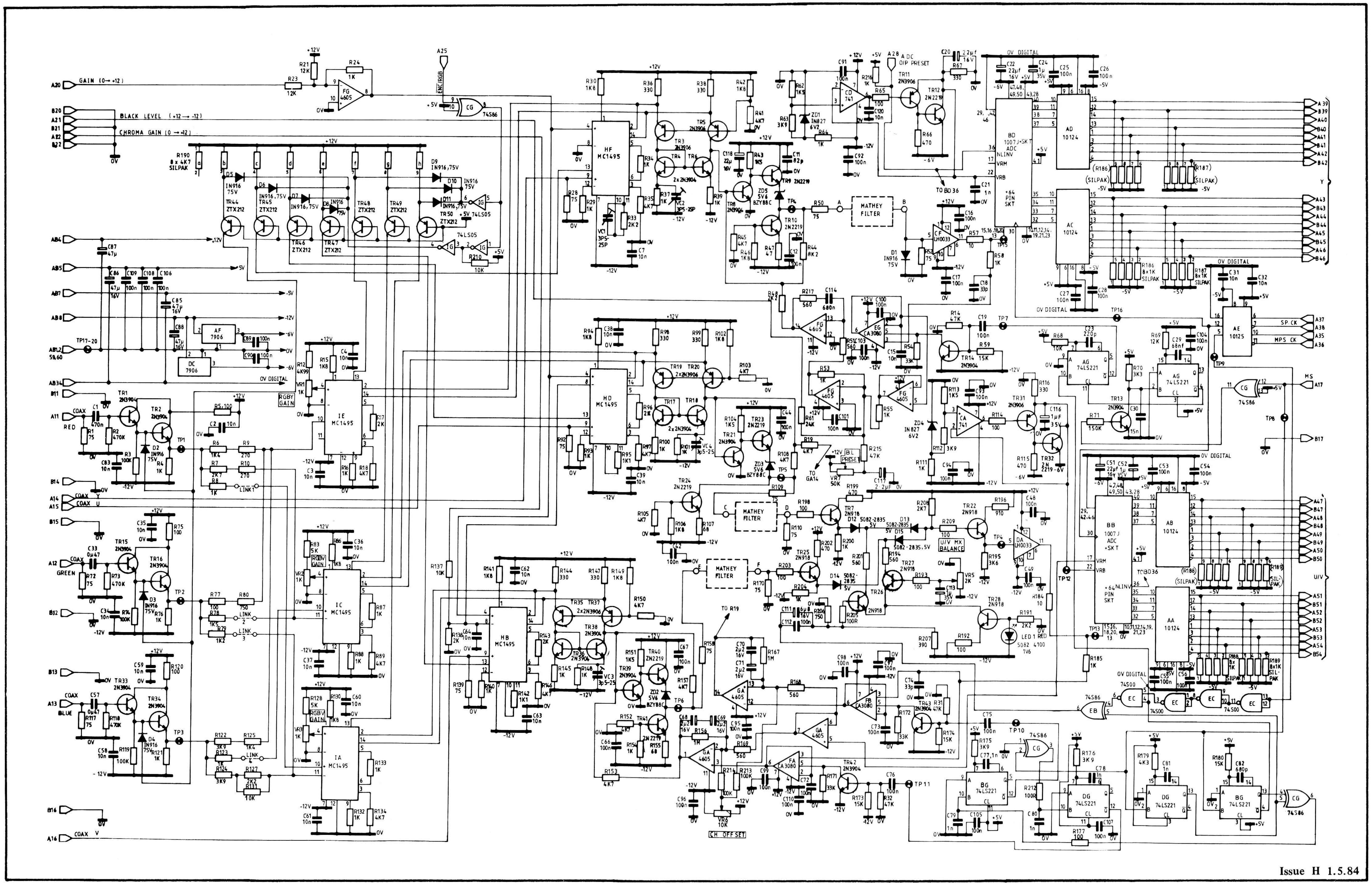
TP31
TP1
TP2
TP3



17402, Figure 2 ADC Card : Circuit Diagram and Component Layout

OUTPUT PROCESSOR CARD

17490 (PAL)

1. INTRODUCTION

This takes digital YUV picture data and converts it into two sets of coded and RGB analogue video output.

2. CIRCUIT DESCRIPTION

Eight bit luminance data is received on edge pins A11 to B14 and converted to analogue by DAC IC3. The DAC voltage reference, which is derived from D1 attenuated and buffered by IC30, TR1, etc., is also used by the chrominance DACs and the blankers.

Eight bit multiplexed R-Y/B-Y data arrives on edge pins A15 to B18 and is demultiplexed by alternately clocking the input latches of the R-Y and B-Y DACs ICs 5 and 4 respectively. D-type flip flop IC2 retimes MPX CLOCK to ensure its correct relationship to sample CK.

The luminance signal from the DAC is blanked by the multiplier IC6. TTL mixed blanking is level shifted and buffered by TR4 to drive TR5 and the chrominance blankers TR23 and TR29 before being shaped by the filter L1, C7, C8, R153 and fed into the Y+ input of the multiplier. VR31 sets the unblanked value of Y+, and is thus the luminance gain control, while VR1 sets the value of Y− to balance the modulator to black during blanking, the black level being set by VR2.

The differential current output of IC6 is converted to 'single ended' volts by the combination of TR2 and TR3 and Video Op Amp IC9.

The colour difference signals B-Y and R-Y are blanked in the same manner by IC7, 10 and IC8, 11 respectively. SW1, 2 and 3 cause Y, B-Y or R-Y to be permanently blanked for setting-up purposes.

The outputs of the three blankers (Y, R-Y, B-Y) are passed through low pass reconstruction filters one 5.5MHz for luminance and two 2.5MHz for R-Y and B-Y. Each filter includes sin x/x correction and the luminance filter also includes a 155ns lumped delay line to adjust chrominance/luminance delay.

The outputs of the filters are level shifted to approximately −1.4V by R's and then buffered by ICs 12, 13 and 14. The outputs of these buffers feed both the coder and inverse RGB matrix.

The RGB matrix consists of three transimpedance amplifiers, each of which has an inverting and non-inverting current input. The output is the difference in the input currents multiplied by the transimpedance set by R184 and VR21 (for green). Each amplifier has adjustments for gain, offset, and colour balance as below.

AMPLIFIER	OFFSET	GAIN	MATRIX
Red	VR26	VR25	VR18
Green	VR22	VR21	VR30 and VR24
Blue	VR27	VR28	VR12

Table 1 RGB Adjustments

The coder is centred around another transimpedance amplifier (TR6 to 12 etc.). This amplifier combines luminance, modulated chrominance and syncs to provide a composite output which is filtered by 65MHz low pass filter to remove harmonics of subcarrier, then amplified by a distribution amplifier (TR18, 19, 20) to provide two 75Ω outputs at edge connector pins A36 and A37.

R-Y is added to burst gate and modulated onto its subcarrier by IC17 and IC18. Burst gate is derived from TTL burst gate by switched current sources TR26 and TR30. L5, C71 and C72 shape the edges of burst to provide the correct rise time, modulator balance is controlled by VR15 and gain by VR16.

B-Y is modulated in a similar manner by ICs 15 and 16, burst gate coming from TR25 and TR26. Balance is controlled by VR9 and gain by VR29.

The combined output of the modulators is fed into the mixer amplifier via capacitors C113, C114. U and V subcarrier is made by 'clocking' one phase of TTL subcarrier on two successive edges of TTL 4 x subcarrier (17.433MHz) using IC20. V subcarrier has ident applied by Ex-OR gate IC21. To achieve complementary drive for the double balanced modulators a TTL to ECL convertor is used (IC 125).

TTL syncs are processed and shaped in a similar manner to burst gate by TR17, L8 etc., before they are inverted and amplified by IC29 for use with RGB OUT. TR13 to 16 form a differential amplifier to feed syncs for the coded output into the mixer amplifier as differential current.

CAPACITORS

REF.	DESCRIPTION	STOCK CODE
C1	6.8μF, 16V, 20%	03/03/013X
C2	100000pF, 50V, +80%-20%	03/06/0233
C3	6.8μF, 16V, 20%	03/03/013X
C4, C5	1μF, 35V, 20%	03/03/004Y
C6	6.8pF, 100V	03/06/0543
C7	270pF, 100V, 10%	03/06/0349
C8	120pF, 100V, 10%	03/01/0414
C9, C10	10pF, 100V, 10%	03/06/0012
C11-C14	100000pF, 50V, +80%-20%	03/06/0233
C15	2.7pF, 63V	03/00/0176
C16	10000pF, 100V, +80%-20%	03/06/0101
C17	100000pF, 50V, +80%-20%	03/06/0233
C18	6.8μF, 25V, 20%	03/03/0148
C19	100000pF, 50V, +80%-20%	03/06/0233
C20	6.8μF, 25V, 20%	03/03/0148
C21	270pF, 100V,10%	03/06/0349
C22	47pF, 100V, 10%	03/06/0047
C23	2.7pF, 63V	03/00/0176
C24	100000pF, 50V, +80%-20%	03/06/0233
C25	10000pF, 100V, +80%-20%	03/06/0101
C26	100000pF, 50V, +80%-20%	03/06/0233
C27	6.8μF, 16V, 20%	03/03/013X
C28	100000pF, 50V, +80%-20%	
C29	6.8μF, 16V, 20%	03/03/013X
C30, C31	1μF, 35V, 20%	03/03/004Y
C32	270pF, 100V,10%	03/06/0349
C33	120pF, 100V, 10%	03/01/0414
C34-C36	10pF, 100V, 10%	03/06/0012
C37	100000pF, 50V, +80%-20%	03/06/0233
C38	10pF, 100V, 10%	03/06/0012
C39	100000pF, 50V, +80%-20%	03/06/0233
C40	NOT FITTED	
C41-C45	10000pF, 100V, +80%-20%	03/06/0101
C46	270pF, 100V, 10%	03/06/0349
C47	47pF, 100V, 10%	03/06/0047
C48	NOT FITTED	
C49	6.8μF, 16V, 20%	03/03/013X
C50	100000pF, 50V, +80%-20%	03/06/0233
C51	6.8μF, 16V, 20%	03/03/013X
C52	1μF, 35V, 20%	03/03/004Y
C53	270pF, 100V, 10%	03/06/0349
C54	120pF, 100V, 10%	03/01/0414
C55	1μF, 35V, 20%	03/03/004Y
C56-C58	10pF, 100V, 10%	03/06/0012
C59, C60	100000pF, 50V, +80%-20%	03/06/0233
C61	10pF, 100V, 10%	03/06/0012
C62	10000pF, 100V, +80%-20%	03/06/0101
C63	NOT FITTED	
C64, C65	10000pF, 100V, +80%-20%	03/06/0101
C66	NOT FITTED	

CAPACITORS (Cont.)

REF.	DESCRIPTION	STOCK CODE
C67	10000pF, 100V, +80%-20%	03/06/0101
C68‘ C69	NOT FITTED	
C70	AOT	
C71	270pF, 100V, 10%	03/06/0349
C72	47pF, 100V, 10%	03/06/0047
C73	47μF, 25V, 20%	03/03/030X
C74	6.8μF, 35V, 20%	03/03/0156
C75	100000pF, 50V, +80%-20%	03/06/0233
C76	47μF, 25V, 20%	03/03/030X
C77	NOT FITTED	
C78, C79	47μF, 25V, 20%	03/03/030X
C80	6.8μF, 35V, 20%	03/03/0156
C81	100000pF, 50V, +80%-20%	03/06/0233
C82	2.7pF, 63V	03/00/0176
C83	10000pF, 100V, +80%-20%	03/06/0101
C84	6.8μF, 25V, 20%	03/03/0148
C85, C86	100000pF, 50V, +80%-20%	03/06/0233
C87	6.8μF, 25V, 20%	03/03/0148
C88	2.7pF, 63V	03/00/0176
C89	10000pF, 100V, +80%-20%	03/06/0101
C90	100000pF, 50V, +80%-20%	03/06/0233
C91	6.8μF, 25V, 20%	03/03/0148
C92	100000pF, 50V, +80%-20%	03/06/0233
C93	6.8μF, 25V, 20%	03/03/0148
C94	2.7pF, 53V	03/00/0176
C95	10000pF, 100V, +80%-20%	03/06/0101
C96	100000pF, 50V, +80%-20%	03/06/0233
C97	6.8μF, 25V, 20%	03/03/0148
C98	100000pF, 50V, +80%-20%	03/06/0233
C99	6.8μF, 25V, 20%	03/03/0148
C100, C101	NOT FITTED	
C102	2.2pF, 63V	03/01/0015
C103	100000pF, 50V, +80%-20%	03/06/0233
C104	1μF, 35V, 20%	03/03/004Y
C105	100000pF, 50V, +80%-20%	03/06/0233
C106	1μF, 35V, 20%	03/03/004Y
C107	100000pF, 50V, +80%-20%	03/06/0233
C108	1μF, 35V, 20/	03/03/004Y
C109-C112	100000pF, 50V, +80%-20%	03/06/0233
C113, C114	120pF, 100V, 10%	03/01/0414
C115, C116	NOT FITTED	
C117, C118	82pF, 100V, 20%	03/06/0624
C119	82pF, 100V, 20%	03/06/0624
VC1, VC2	3.5pF-25pF, 50V	03/07/0212

RESISTORS

REF.	DESCRIPTION	STOCK CODE
R1	560Ω, 250mW, 1%, 50ppm	01/01/0581

REF.	DESCRIPTION	STOCK CODE
RESISTORS (Cont.)		
R2	1.2kΩ, 250mW, 1%, 50ppm	01/01/2061
R3	6.2kΩ, 250mW, 1%, 50ppm	01/01/0891
R4	1kΩ, 250mW, 1%, 50ppm	01/01/0638
R5, R6	100Ω, 250mW, 1%, 50ppm	01/01/0328
R7	NOT FITTED	
R8	3.9kΩ, 250mW, 1%, 50ppm	01/01/2142
R9	3.3kΩ, 250mW, 1%, 50ppm	01/01/2134
R10	10kΩ, 250mW, 1%, 50ppm	01/01/2207
R11	1kΩ, 250mW, 1%, 50ppm	01/01/0638
R12	100Ω, 250mW, 1%, 50ppm	01/01/0328
R13	3.9kΩ, 250mW, 1%, 50ppm	01/01/2142
R14, R15	22kΩ, 250mW, 1%, 50ppm	01/01/2231
R16	220Ω, 250mW, 1%, 50ppm	01/01/0441
R17, R18	4.7kΩ, 125mW, 0.1%, 50ppm	01/03/0981
R19	NOT FITTED	
R20	1.8kΩ, 250mW, 1%, 50ppm	01/01/2088
R21	2.2kΩ, 250mW, 1%, 50ppm	01/01/0727
R22	22kΩ, 250mW, 1%, 50ppm	01/01/2231
R23, R24	2kΩ, 250mW, 1%, 50ppm	01/01/2096
R25	2.4kΩ, 250mW, 1%, 50ppm	01/01/210X
R26	1.5kΩ, 250mW, 1%, 50ppm	01/01/207X
R27	470Ω, 250mW, 1%, 50ppm	01/01/0557
R28	10kΩ, 125mW, 0.1%, 50ppm	01/03/1139
R29	75Ω, 250mW, 1%, 50ppm	01/01/0255
R30	10kΩ, 125mW, 0.1%, 50ppm	01/03/1139
R31	75Ω, 250mW, 1%, 50ppm	01/01/0255
R32	470Ω, 250mW, 1%, 50ppm	01/01/0557
R33, R34	100%, 250mW, 1%, 50ppm	01/01/0328
R35	1.5kΩ, 250mW, 1%, 50ppm	01/01/207X
R36	6.2kΩ, 250mW, 1%, 50ppm	01/01/0891
R37	1.2kΩ, 250mW, 1%, 50ppm	01/01/2061
R38	6.2kΩ, 250mW, 1%, 50ppm	01/01/891P
R39	1kΩ, 250mW, 1%, 50ppm	01/01/0638
R40	2.4kΩ, 250mW, 1%, 50ppm	01/01/210X

REF.	DESCRIPTION	STOCK CODE
RESISTORS (Cont.)		
R41, R42	1kΩ, 250mW, 1%, 50ppm	01/01/0638
R43	47Ω, 250mW, 1%, 50ppm	01/01/0204
R44	3.3kΩ, 250mW, 1%, 50ppm	01/01/2134
R45	75Ω, 250mW, 1%, 50ppm	01/01/0255
R46-R48	4.7kΩ, 250mW, 1%,	01/01/2177
R49	6.8kΩ, 250mW, 1%, 50ppm	01/01/0905
R50	3.9kΩ, 250mW, 1%, 50ppm	01/01/2142
R51	1kΩ, 250mW, 1%, 50ppm	01/01/0638
R52, R53	3.3kΩ, 250mW, 1%, 50ppm	01/01/2134
R54	470Ω, 250mW, 1%, 50ppm	01/01/0557
R55	1kΩ, 250mW, 1%, 50ppm	01/01/0638
R56	75Ω, 250mW, 1%, 50ppm	01/01/0255
R57	1kΩ, 250mW, 1%, 50ppm	01/01/0638
R58	1.5kΩ, 250mW, 1%, 50ppm	01/01/207X
R59	2kΩ, 250mW, 1%, 50ppm	01/01/2096
R60	3.3kΩ, 250mW, 1%, 50ppm	01/01/2134
R61	47Ω, 250mW, 1%, 50ppm	01/01/0204
R62, R63	75Ω, 250mW, 1%, 50ppm	01/01/0255
R64	10kΩ, 250mW, 1%, 50ppm	01/01/2207
R65	33kΩ, 250mW, 1%, 50ppm	01/01/1057
R66	75Ω, 250mW, 1%, 50ppm	01/01/0255
R67	1.2kΩ, 250mW, 1%, 50ppm	01/01/2061
R68	3.3kΩ, 250mW, 1%, 50ppm	01/01/2134
R69	1kΩ, 250mW, 1%, 50ppm	01/01/0638
R70	10kΩ, 250mW, 1%, 50ppm	01/01/2207
R71	560Ω, 250mW, 1%, 50ppm	01/01/0581
R72	NOT FITTED	
R73	1kΩ, 250mW, 1%, 50ppm	01/01/0638
R74	220Ω, 250mW, 1%, 50ppm	01/01/0441
R75	1.8kΩ, 250mW, 1%, 50ppm	01/01/2088
R76	5.6kΩ, 250mW, 1%, 50ppm	01/01/255X
R77	15kΩ 250mW, 1%, 50ppm	01/01/2223
R78, R79	470Ω, 125mW, 0.1%, 50ppm	01/03/040X
R80	470Ω, 250mW, 1%, 50ppm	01/01/0557

17490 Component List (Cont.)

RESISTORS (Cont.)

REF.	DESCRIPTION	STOCK CODE
R81	1.8kΩ, 250mW, 1%, 50ppm	01/01/2088
R82, R83	2.25kΩ, 125mW, 0.1%, 50ppm	01/03/2275
R84	470Ω, 250mW, 1%, 50ppm	01/01/0557
R85, R86	3.3kΩ, 250mW, 1%, 50ppm	01/01/2134
R87	1.2kΩ, 250mW, 1%, 50ppm	01/01/2061
R88	47Ω, 250mW, 1%, 50ppm	01/01/0204
R89, R90	75Ω, 250mW, 1%, 50ppm	01/01/0255
R91	NOT FITTED	
R92	470Ω, 250mW, 1%, 50ppm	01/01/0557
R93	750Ω, 250mW, 1%, 50ppm	01/01/2053
R94	3.3kΩ, 250mW, 1%, 50ppm	01/01/2134
R95	470Ω, 250mW, 1%, 50ppm	01/01/0557
R96, R97	1kΩ, 250mW, 1%, 50ppm	01/01/0638
R98, R99	10kΩ, 250mW, 1%, 50ppm	01/01/2207
R100	5.6kΩ, 250mW, 1%, 50ppm	01/01/255X
R101	470Ω, 250mW, 1%, 50ppm	01/01/0557
R103, R103	5.6kΩ, 250mW, 1%, 50ppm	01/01/255X
R104	NOT FITTED	
R105	3.9kΩ, 250mW, 1%, 50ppm	01/01/2142
R106	1.1kΩ, 250mW, 1%, 50ppm	01/01/0654
R107	120Ω, 250mW, 1%, 50ppm	01/01/0352
R108	2.2kΩ, 250mW, 1%, 50ppm	01/01/0727
R109	75Ω, 250mW, 1%, 50ppm	01/01/0255
R110	1kΩ x 7, 125mW, 5%, 300ppm	01/08/206X
R111	1kΩ, 250mW, 1%, 50ppm	01/01/0638
R112	NOT FITTED	
R113	470Ω, 250mW, 1%, 50ppm	01/01/0557
R114, R115	1kΩ, 250mW, 1%, 50ppm	01/01/0638
R116	220Ω, 250mW, 1%, 50ppm	01/01/0441
R117	1kΩ, 250mW, 1%, 50ppm	01/01/0638
R118	470Ω, 250mW, 1%, 50ppm	01/01/0557
R119	NOT FITTED	
R120	120Ω, 250mW, 1%, 50ppm	01/01/0352
R121	1.2kΩ, 250mW, 1%, 50ppm	01/01/2061
R122	3.3kΩ, 250mW, 1%, 50ppm	01/01/2134
R123	NOT FITTED	

RESISTORS (Cont.)

REF.	DESCRIPTION	STOCK CODE
R125	560Ω, 250mW, 1%, 50ppm	01/01/0581
R126, R127	NOT FITTED	
R128	220Ω, 250mW, 1%, 50ppm	01/01/0441
R129	1.8kΩ, 250mW, 1%, 50ppm	01/01/2088
R130	5.6kΩ, 250mW, 1%, 50ppm	01/01/255X
R131	15kΩ, 250mW, 1%, 50ppm	01/01/2223
R132, R133	470Ω, 125mW, 0.1%, 50ppm	01/03/2275
R134	470Ω, 250mW, 1%, 50ppm	01/01/0557
R135	2.25kΩ, 125mW, 0.1%, 50ppm	01/03/2275
R136	1.8kΩ, 250mW, 1%, 50ppm	01/01/2088
R137	2.25kΩ, 125mW, 0.1%, 50ppm	01/03/2275
R138	470Ω, 250mW, 1%, 50ppm	01/01/0557
R139, R140	3.3kΩ, 250mW, 1%, 50ppm	01/01/2134
R141	1.2kΩ, 250mW, 1%, 50ppm	01/01/2061
R142	NOT FITTED	
R143, R144	75Ω, 250mW, 1%, 50ppm	01/01/0255
R145	3.3kΩ, 250mW, 1%, 50ppm	01/01/2134
R146, R147	NOT FITTED	
R148-R150	470Ω, 250mW, 1%, 50ppm	01/01/0557
R151, R152	1kΩ, 250mW, 1%, 50ppm	01/01/0638
R153, R154	820Ω, 250mW, 1%, 50ppm	01/01/0611
R155	470Ω, 250mW, 1%, 50ppm	01/01/0557
R156	1kΩ, 250mW, 1%, 50ppm	01/01/0638
R157	10kΩ, 250mW, 1%, 50ppm	01/01/2207
R158	5.1kΩ, 250mW, 1%, 50ppm	01/01/0867
R159	820Ω, 250mW, 1%, 50ppm	01/01/0611
R160	470Ω, 250mW, 1%, 50ppm	01/01/0557
R161, R162	5.6kΩ, 250mW, 1%, 50ppm	01/01/255X
R163	1.5kΩ, 250mW, 1%, 50ppm	01/01/207X
R164	1.2kΩ, 250mW, 1%, 50ppm	01/01/2061
R165	470Ω, 250mW, 1%, 50ppm	01/01/0557
R166	1kΩ, 250mW, 1%, 50ppm	01/01/0638
R167	6.2kΩ, 250mW, 1%, 50ppm	01/01/0891
R168	560Ω, 250mW, 1%, 50ppm	01/01/0581
R169	470Ω, 250mW, 1%, 50ppm	01/01/0557

17490 Component List (Cont.)

RESISTORS (Cont.)

REF.	DESCRIPTION	STOCK CODE
R170	1kΩ, 250mW, 1%, 50ppm	01/01/0638
R171	1.2kΩ, 250mW, 1%, 50ppm	01/01/2061
R172	75Ω, 250mW, 1%, 50ppm	01/01/0255
R173	2.7kΩ, 250mW, 1%, 50ppm	01/01/2126
R174	6.2kΩ, 250mW, 1%, 50ppm	01/01/0891
R175, R176	NOT FITTED	
R177	3.3kΩ, 250mW, 1%, 50ppm	01/01/2134
R178	NOT FITTED	
R179	47Ω, 250mW, 1%, 50ppm	01/01/0204
R180, R181	100Ω, 250mW, 1%, 50ppm	01/01/0328
R182	1.5kΩ, 250mW, 1%, 50ppm	01/01/207X
R183	6.2kΩ, 250mW, 1%, 50ppm	01/01/0891
R184	2.4kΩ, 250mW, 1%, 50ppm	01/01/210X
R185-R189	1kΩ, 250mW, 1%, 50ppm	01/01/0638
R190	47Ω, 250mW, 1%, 50ppm	01/01/0204
R191	3.3kΩ, 250mW, 1%, 50ppm	01/01/2134
R192	75Ω, 250mW, 1%, 50ppm	01/01/0255
R193, R194	100Ω, 250mW, 1%, 50ppm	01/01/0328
R195	1.5kΩ, 250mW, 1%, 50ppm	01/01/207X
R196	6.2kΩ, 250mW, 1%, 50ppm	01/01/0891
R197	2.4kΩ, 250mW, 1%, 50ppm	01/01/210X
R198, R199	1kΩ, 250mW, 1%, 50ppm	01/01/0638
R200	120Ω, 250mW, 1%, 50ppm	01/01/0352
R201	180Ω, 250mW, 1%, 50ppm	01/01/2002
R202	680Ω, 250mW, 1%, 50ppm	01/01/2045
R203	6.2kΩ, 250mW, 1%, 50ppm	01/01/0891
R204	1kΩ, 250mW, 1%, 50ppm	01/01/0638
R205	2.2kΩ, 250mW, 1%, 50ppm	01/01/0727
R206-R208	1.5kΩ, 250mW, 1%, 50ppm	01/01/207X
R209, R210	NOT FITTED	
R211	5.6kΩ, 210mW, 2%, 100ppm	01/12/0107
R212, R213	560Ω, 250mW, 1%, 50ppm	01/01/0581
R214, R215	1kΩ, 250mW, 1%, 50ppm	01/01/0638
R216	5.1kΩ, 250mW, 1%, 50ppm	01/01/0867
R217-R219	75Ω, 250mW, 1%, 50ppm	01/01/0255

RESISTORS (Cont.)

REF.	DESCRIPTION	STOCK CODE
R220	470Ω, 250mW, 1%, 50ppm	01/01/0557
R221	1.2kΩ, 250mW, 1%, 50ppm	01/01/2061
R222	AOT	
R223	560Ω, 250mW, 1%, 50ppm	01/01/0581
R224	75Ω, 250mW, 1%, 50ppm	01/01/0255
VR1	20kΩ, 50mW, 10%	02/02/0084
VR2	200Ω, 50mW, 10%	02/02/0025
VR3	5kΩ, 50mW, 10%	02/05/0269
VR4	500Ω, 50mW, 10%	02/05/025Y
VR5	2kΩ, 50mW, 10%	02/03/0039
VR6	20kΩ, 50mW, 10%	02/02/0084
VR7	200Ω, 50mW, 10%	02/02/0025
VR8	NOT FITTED	
VR9	200Ω, 50mW, 10%	02/05/0226
VR10	10kΩ, 50mW, 10%	02/03/0055
VR11	1kΩ, 50mW, 10%	02/05/0277
VR12	200Ω, 50mW, 10%	02/02/0025
VR13	20kΩ, 50mW, 10%	02/)2/0084
VR14	200Ω, 50mW, 10%	02/02/0025
VR15	200Ω, 50mW, 10%	02/05/0226
VR16	500Ω, 50mW, 10%	02/05/025Y
VR17	NOT FITTED	
VR18	200Ω, 50mW, 10%	02/02/0025
VR19, VR20	NOT FITTED	
VR21	500Ω, 50mW, 10%	02/02/0033
VR22	5kΩ, 50mW, 10%	02/02/0068
VR23	NOT FITTED	
VR24	1kΩ, 50mW, 10%	02/02/0041
VR25	500Ω, 50mW, 10%	02/02/0033
VR26, VR27	5kΩ, 50mW, 10%	02/02/0068
VR28	500Ω, 50mW, 10%	02/02/0033
VR29	500Ω, 50mW, 10%	02/05/025Y
VR30	1kΩ, 50mW, 10%	02/02/0041
VR31, VR32	2kΩ, 50mW, 10%	02/03/0039

SEMICONDUCTORS

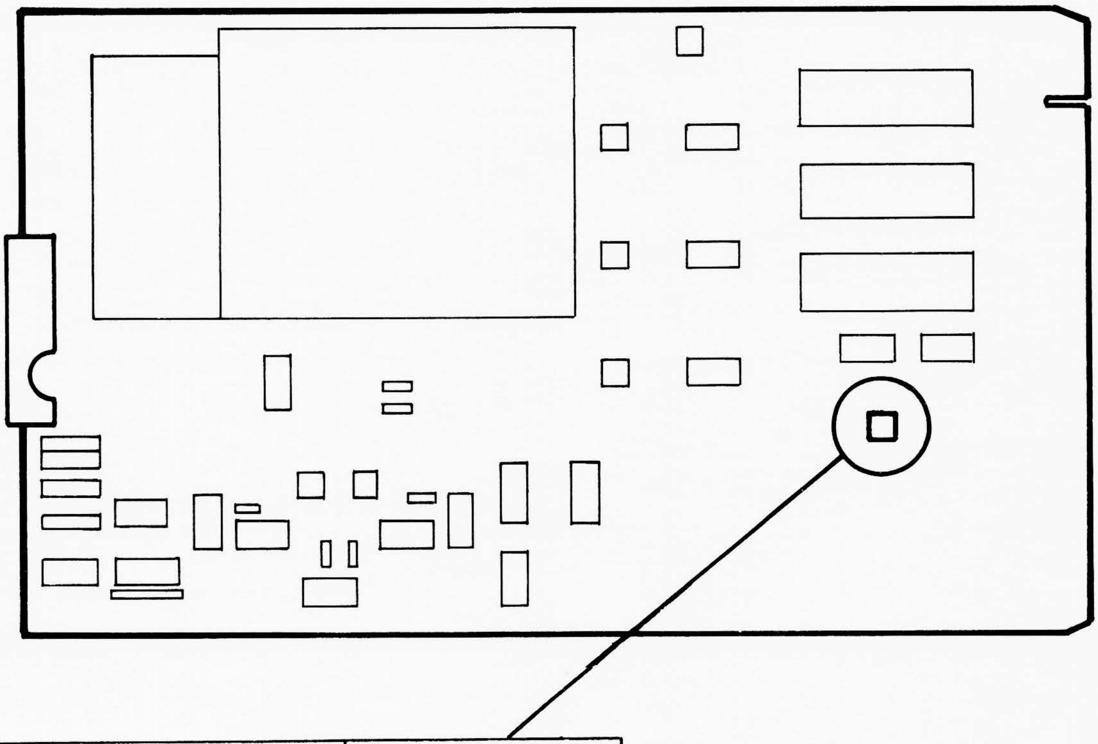
REF.	DESCRIPTION	STOCK CODE
D1	NOT FITTED	
D2-D14	75V, 500mW	06/01/0083
D15, D16	NOT FITTED	
D17-D19	75V, 500mW	06/01/0083
D20	NOT FITTED	
ZD1	6.2V, 400mW	06/02/0062
ZD2	3.0V, 500mW	06/02/0119
ZD3	5.6V, 500mW	06/02/0208
ZD4, ZD5	2.7V, 500mW	06/02/0151
ZD6-ZD10	5.6V, 500mW	06/02/0208
TR1	PNP 2N2905 60V	05/01/0063
TR2	NOT FITTED	
TR3	PNP MD3251 40V	05/05/0057
TR4	PNP 2N3906 40V	05/01/0403
TR5	NPN 2N3904 60V	05/01/0667
TR6, TR7	PNP 2N3906 40V	05/01/0403
TR8-TR10	NPN 2N3904 60V	05/01/0667
TR11, TR12	NPN 2N2219 60V	05/01/0039
TR13-TR17	PNP 2N3906 40V	05/01/0403
TR18	NPN 2N3904 60V	05/01/0667
TR19	NOT FITTED	

17490 Component List (Cont.)

REF.	DESCRIPTION	STOCK CODE
SEMICONDUCTORS (Cont.)		
TR20, TR21	NPN 2N2219 60V	05/01/0039
TR22	PNP MD3251 40V	05/05/0057
TR23	NPN 2N3904 60V	05/01/0667
TR24	NOT FITTED	
TR25	PNP 2N3906 40V	05/01/0403
TR26	NPN 2N3904 60V	05/01/0667
TR27	NOT FITTED	
TR28	PNP MD3251 40V	05/05/0057
TR29	NPN 2N3904 60V	05/01/0667
TR30-TR32	PNP 2N3906 40V	05/01/0403
TR33-TR35	NPN 2N3905 60V	05/01/0667
TR36, TR37	NPN 2N2219 50V	05/01/0039
TR38, TR39	PNP 2N3906 40V	05/01/0403
TR40-TR42	NPN 2N3904 60V	05/01/0667
TR43, TR44	NPN 2N2219 60V	05/01/0039
TR45, TR46	PNP 2N3906 40V	05/01/0403
TR47-TR49	NPN 2N3904 60V	05/01/0667
TR50, TR51	NPN 2N2219 60V	05/01/0039
TR52, TR53	NOT FITTED	
TR54	PNP 2N3906 40V	05/01/0403
INTEGRATED CIRCUITS		
AJ	10124P	04/01/207Y
AK	74S86N	04/01/207Y
BF	3045	04/03/1881
BG, BH	3054	04/03/3973
BI	3045	04/03/1881

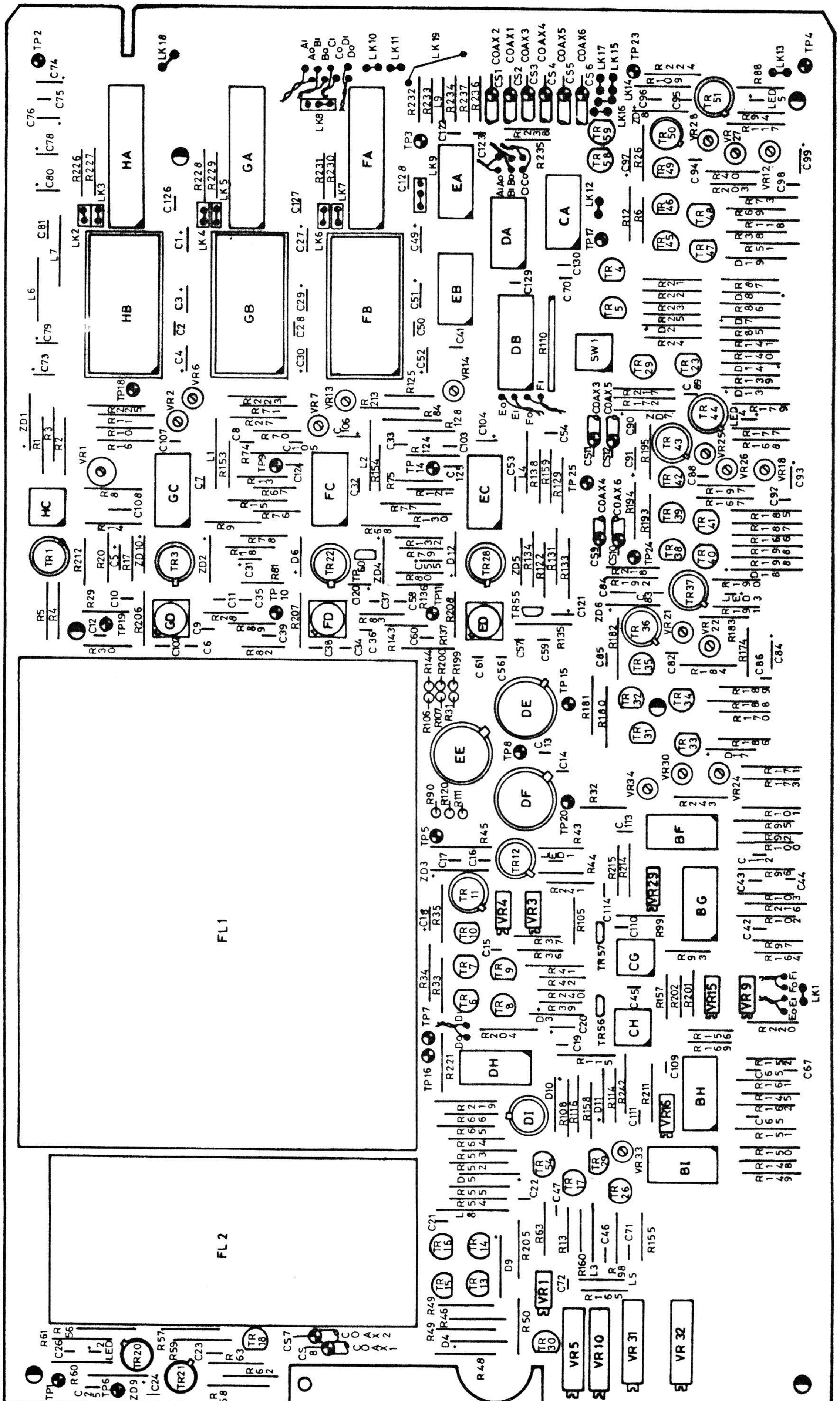
REF.	DESCRIPTION	STOCK CODE
INTEGRATED CIRCUITS (Cont.)		
BJ	74S74N	04/01/0698
DE, DF	0033CG	04/02/0111
DH	7416N	04/01/0353
DI	3507J	04/02/012X
EA	74S74N	04/01/0698
EB	74S04N	07/02/0015
EC	1495L	04/01/1902
ED	0024CH	04/02/0103
EE	0033CG	04/02/0111
FA	Dil Switch	29/01/025Y
FC	1495L	04/01/1902
FD	0024CH	04/02/0103
GA	Dil Switch	29/01/025Y
GC	1495L	04/01/1902
GD	0024CH	04/02/0103
HA	Dil Switch	29/01/025Y
HC	741CN	04/01/250X
MISCELLANEOUS		
L1-L5	Inductor 47μH, 235mA, 10%	07/01/0141
L6, L7	Coil	07/02/0015
L8	Inductor 47μH, 235mA, 10%	07/01/0141
LED1-5	Light Emitting Diode Red	06/03/030Y

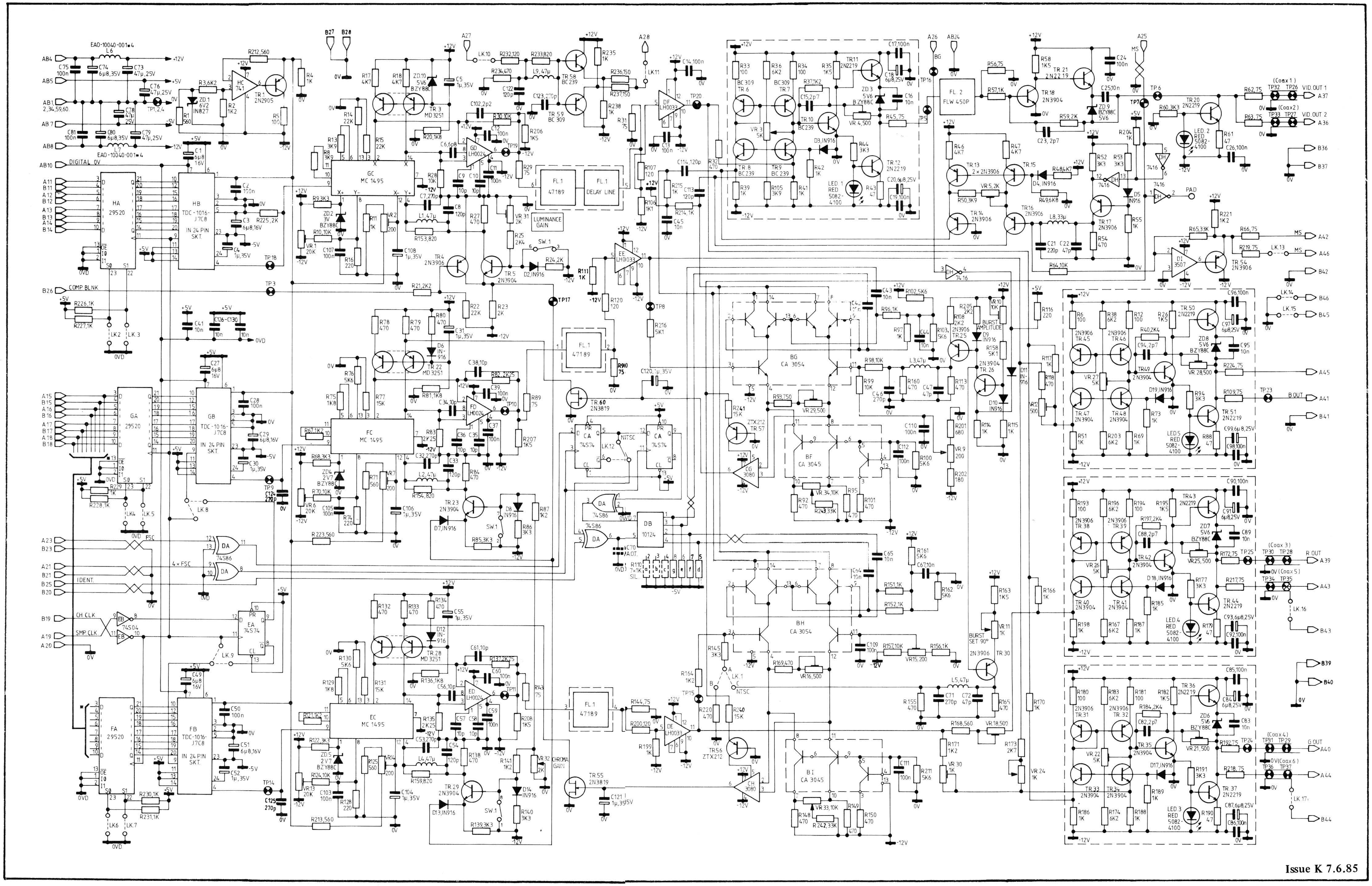
17490 Component List (Cont.)



	1	2	3	4
DISABLE R-Y	ON			
DISABLE B-Y		ON		
DISABLE Y			ON	
UNUSED				-
STANDARD CONFIGURATION	OFF	OFF	OFF	OFF

17490, Figure 1 Output Processor Card Switch Configurations


17490
HA
GA
FA
EA
DA
CA
HB
GB
FB
EB
DB
HC
GC
FC
EC
GD
FD
ED
DE
EE
DF
FL1
FL 2
BF
BG
CG
CH
DH
DI
BH
BI
SW1
TP1
TP2
TP3
TP4
TP5
TP6
TP7
TP8
TP11
TP15
TP16
TP17
TP18
TP19
TP20
TP23
TP24
TP25
LK1
LK2
LK3
LK4
LK5
LK6
LK7
LK8
LK9
LK10
LK11
LK12
LK13
LK14
LK15
LK16
LK17
LK18
LK19
COAX 1
COAX 2
COAX 3
COAX 4
COAX 5
COAX 6
CS1
CS2
CS3
CS4
CS5
CS6
CS7
VR1
VR2
VR3
VR4
VR5
VR6
VR7
VR9
VR10
VR12
VR13
VR14
VR15
VR16
VR18
VR21
VR22
VR24
VR25
VR26
VR27
VR28
VR29
VR30
VR31
VR32
VR33
VR34
TR1
TR3
TR4
TR5
TR22
TR28
TR29
TR23
TR36
TR37
TR44
TR51
TR55
TR56
TR57
FL1
FL 2



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17490, Figure 2 Output Processor Card : Circuit Diagram and Component Layout

CHROMA SEPARATOR CARD

17413

1 CIRCUIT DESCRIPTION

The purpose of the Chroma Separator card is to divide the composite PAL video input into pure luminance and pure chrominance components and also to demodulate the chrominance components to R-Y and B-Y base band signals. This card operates in conjunction with the two Video Delay cards 17462 which provide three signals to the Chroma Separators. These signals are firstly, an undelayed video input at pin AB50, the video input delayed by one television line at pin AB52 and the video input delayed by two television lines at pin AB54. The only other externally derived input to this card is the burst gate pulse on pin AB25. The following circuit description assumes that the Video Delay cards have been adjusted such that the three video signals appearing at test points 5, 6 and 12 are all equal in amplitude have identical frequency response and are delayed by 0, 1 line and 2 lines respectively. Complete separation of luminance and chrominance may be achieved by matrixing suitably band limited components from the three video signals appearing at TP5, TP6 and TP12. This is made possible because the subcarrier frequency used to carry the chrominance information reverses in phase after two television lines in the PAL system. For the following explanation we will call the signal at TP6 the 'middle line' and the signal at TP5 and TP12 we will call the 'outer lines'. The luminance and colour difference information finally generated at the output of this circuit is derived mostly from the middle line.

2. LUMINANCE SEPARATION

Addition of the two outer line signals at the wiper of VR14 causes the chrominance components from these lines to cancel resulting in a vertically averaged pure luminance signal. This signal is applied to the base of TR1, and the composite video from the middle line is applied to the base of TR2. TR1 and TR2 in conjunction with L1, R13 and capacitors C3 and VC1 form a band pass differential amplifier which transmits only the difference signals between the bases of TR1 and TR2 which fall within the pass band defined by the tuned circuit. As there is no chrominance in the signal appearing at the wiper of VR14 the differential amplifier sense the chrominance components at the base of TR2 and it is this which is transmitted via transformer T1 and TP9. It should be noted that this chrominance is derived from the middle line.

Delay line EB compensates for the signal delay through the tuned circuit L1, C3 and VC1 and provides the subtractor TR6 and TR5 with a complete composite video input at the base of TR6. The chrominance signal at the base of TR5 is subtracted from the composite video input at TR6 in the resistor network R26, R28 and VR3. VR3 may also be adjusted to set up the subtractor levels.

The feedback amplifier FA increases the luminance level to approximately 1V as it leaves the circuit L2, C6, VC4 and VR5 form a narrow band notch circuit operating at chrominance frequency to remove any residual chrominance which has bot been completely eliminated by the matrixing circuits.

Delay line DL1 compensates for the increased delay through the chrominance path and is adjusted to minimise chrominance/luminance delay in the decoded signals.

3. CHROMINANCE SEPARATION

We have already seen that adding the video signals from the outer lines provides a pure luminance signal; subtracting these PAL video signals will therefore provide pure chrominance. TR10 and TR11 in conjunction with current sources TR8 and TR7 form a differential amplifier which subtract the video signals from the outer lines. Band pass filter components L3, R42, C12 and VC5 ensure that only chrominance components are subtracted. The curcuit is not sensitive to low frequency information. The collector currents of TG10 and TR11 respond only to the chrominance information from the video inputs and are 180° out of phase with respect to each other. Chrominance from the middle line is available at the emitter of TR5 and this is delayed by a quarter of a subcarrier cycle by delay line GC. This signal is applied to the bases of TR9 and TR12 as an input to these common emitter amplifiers. Collector currents of TR9 and TR12 are therefore derived from the base voltages at TR9 and TR12 and also the collector currents of TR10 and TR11. These two transistors TR9 and TR12 can therefore be regarded as sum and difference amplifiers for the chrominance signals from the middle line and the combination of the chrominance from the outer lines TP13 and TP14. We would therefore expect to see the U envelope and the V envelope of the chrominance information.

4. BURST LOCKED OSCILLATOR AND DEMODULATOR

The decoder circuit uses only two mixers for the decoding process and the control of the burst locked reference oscillator. This is achieved by switching the phase of the reference subcarrier to the B-Y demodulator during the burst gate interval.

The demodulator circuit may be divided into three sections,

a) the mixers and amplifiers GE, HE, EE and DE followed by low pass filters and output buffers AE and AD,

b) the reference oscillator and voltage control circuits JD, JE and JF combined with the phase testing network HF, GF and EF.

c) the PAL ident detector circuits CF, DF and EF pins 8 to 10.

The two mixer circuits EE and GE followed by amplifiers DE and HE respectively are identical circuits which demodulate the U and V chrominance components at pins 9 and 12 of the mixers EE and GE which are provided with reference subcarrier at pins 8 and 4. The gain of the demodulators is adjusted by VR9 and VR11 and the resulting base band components B-Y and R-Y are amplified by feedback amplifiers DE and HE.

The resulting difference components B-Y and R-Y are buffered by AE and AD to provide a 75Ω output at pins AB16 and AB18. The B-Y output is also low pass filtered by the network L5, C46, C51, L4 and C50 and further buffered by JE5 to 7 before being applied to the sample and hold circuit formed by switching package JD and the storage capacitor C30. This B-Y information which is sampled during burst interval is now available to control frequency of the crystal oscillator XL1 and JF. Amplifier JE pins 12 to 14 controls the frequency response of the phase locked loop and also provides a suitable capture range and holding range for the loop.

To enable only two mixers to be used in the complete decoder it is necessary to phase shift the reference subcarrier to the B-Y mixer by 90° during the burst interval. This is done by monostable GF in conjunction with exclusive OR EF4 to 6. The exclusive OR chooses either edge of the output from GF pin 5 to trigger GF pin 1 and therefore can phase shift the output of GF pins 4 and 13 by the amount defined by VR8, R47 and C13. Monostable HF pins 5 to 11 provide a compensating delay for HF1 to 15 and the exclusive OR pins EF1 to 3 and EF11 to 13 allow the outputs 4 and 13 of HF to be switched by 180° from line to line to eliminate the PAL ident inversion of the R-Y phase.

5. IDENT DETECTOR

R81 and C37 filter the demodulated R-Y output and this signal is compared with a reference level set by VR13 in comparator CF pins 1 to 8. This comparator is gated by the burst gate pulse such tht demodulated chrominance does not appear at TP7. The JK flip-flop DF pins 1 to 6 is arranged such that if the signal at TP7 is high when the latch is clocked at pin 1, the output at pin 5 will change state. This signal from DF5 controls the function of the exclusive OR EF pins 8 to 10 such that the line square wave generated by DF pins 9 to 13 is either inverted or non-inverted to ensure that the polarity of the demodulated R-Y signal is always correct.

6. ADJUSTMENTS

The following procedure assumes that the signals appearing at TP5, TP6 and TP12 are all equal in amplitude, have identical frequency responses and are delayed by 0, one television line and two television lines respectively.

With a line triggered oscilloscope and a multi-burst signal applied to the video input of the DLS 6001P monitor the base of TR1. Adjust VR14, VC2 and VC3 for minimum multiburst. Now monitor TP9 and adjust VR2 for minimum multiburst.

Having obtained pure chrominance we can now use this signal to subtract from the composite video to obtain pure luminance. This is obtained in the following manner, adjust VR1 to make the d.c. level of FA pin 6 approximately 0V. Apply 100% colour bars to the video input of the DLS 6001P and adjust VR3 and VC1 to minimise the chrominance components at FA pin 6. Monitor the output luminance at TP8. Adjust VR5 for maximum residual chrominance. Adjust VC4 for minimum chroma, then VR5 for minimum chrominance.

The UV separators and demodulators may now be adjusted. Observe TP13 and TP14 on a two beam oscilloscope with 100% colour bars applied to the DLS 6001P video input. Adjust VC5 so that the signals at these test points do not ‘twitter’ on alternate lines. VR6 and VR7 may now be adjusted to provide complete U and V separation and it may be necessary to switch off alternately the U and V components on the signal generator to set up accurately the adjustments of VR6 and VR7.

The outputs of the demodulators may now be adjusted to set the mean d.c. level at TP15 and TP17 to 0V by adjusting VR15 and VR16.

To set up the crystal oscillator TP10 should be shorted to 0V and VC6 adjusted such that the demodulated output at TP15 is ‘running through” the correct frequency at a slow rate (less the two cycles per second error). Remove the short circuit at TP10 and adjust VR8 for a maximum signal at TP15. Check the demodulators at B-Y and R-Y signals at output pins AB16 and AB18 respectively and readjust VR15 and VR16 to ensure that the blanking level is set to 0V ±10mV. The gains of the B-Y and R-Y output may now be adjusted using VR9 and VR11 and set to 800mV peak-to-peak for B-Y and R-Y with a 100% colour bar input applied to the DLS 6001P. VR13 should not require readjustment and is normally set fully counter clockwise.

VC2 and VC3 are factory preset and should not require any adjustments.

Note: The initial assumption made at the beginning of this adjustments procedure that the signals at TP5, TP6 and TP12 were idential and separated by one line increments must be checked before embarking on any adjustments to the Chroma Separator card. If assuming this is found not to be true, reference must be made to our Service Deparment before any attempt is made to adjust the gains and delays of the video delay lines.

REF.	DESCRIPTION	STOCK CODE
CAPACITORS		
C1, C2	10000pF, 100V, +80%-20%	03/06/0101
C3	39pF, 100V, 10%	03/06/0039
C4	10000pF, 100V, +80%-20%	03/06/0101
C5	56pF, 100V, 10%	03/01/043Y
C6	22pF, 100V, 10%	03/06/0381
C7	150pF, 100V, 10%	03/06/0365
C8-C11	10000pF, 100V, +80%-20%	03/06/0101
C12	100000pF, 50V, +80%-20%	03/06/0233
C13	33pF, 100V, 10%	03/06/0489
C14	68pF, 100V, 10%	03/06/0497
C15, C16	6.8μF, 25V, 20%	03/03/0148
C17	AOT	
C18, C19	10000pF, 100V, +80%-20%	03/06/0101
C20	AOT	
C21	10pF, 100V, 10%	03/06/0012
C22	AOT	
C23-C26	10000pF, 100V, +80%-20%	03/06/0101
C27	47pF, 100V, 10%	03/06/0047
C28, C29	1μF, 35V, 20%	03/03/004Y
C30	10000pF, 100V, +80%-20%	03/06/0101
C31	22μF, 16V, 20%	03/03/0253
C32	100000pF, 50V, +80%-20%	03/06/0233
C33	22μF, 16V, 20%	03/03/0253
C34	10000pF, 100V, +80%-20%	03/06/0101
C35	22μF, 16V, 20%	03/03/0253
C36	18pF, 100V, 10%	03/06/0462
C37	270pF, 100V, 10%	03/06/0349
C38	10000pF, 100V, +80%-20%	03/06/0101
C39	47μF, 25V, 20%	03/03/030X
C40	68pF, 100V, 10%	03/06/0497
C41-45	6.8μF, 25V, 20%	03/03/0148
C46	27pF, 100V, 10%	03/06/047Y
C47-C49	6.8μF, 25V, 20%	03/03/0148
C50	270pF, 100V, 10%	03/06/0349
C51	82pF, 100V, 10%	03/01/021X
C52, C53	6.8μF, 25V, 20%	03/03/0148
C54	22μF, 16V, 20%	03/03/0253
C55-C61	100000pF, 50V, +80%-20%	03/06/0233
VC1-VC6	3.5pF-25pF, 50V	03/07/0212
RESISTORS		
R1	15kΩ, 250mW, 2%, 100ppm	01/01/0972
R2	68Ω, 250mW, 2%, 100ppm	01/01/0247
R3, R4	25Ω, 125mW, 0.1%, 50ppm	01/03/0035
R5	100Ω, 250mW, 2%, 100ppm	01/01/0336

REF.	DESCRIPTION	STOCK CODE
RESISTORS (Cont.)		
R6-R8	75Ω, 250mW, 2%, 100ppm	01/01/0263
R9	120Ω, 250mW, 2%, 100ppm	01/01/0352
R10, R11	10kΩ, 250mW, 2%, 100ppm	01/01/0948
R12	2.2kΩ, 250mW, 2%, 100ppm	01/01/1642
R13-R15	1kΩ, 250mW, 2%, 100ppm	01/01/0646
R16	4.7kΩ, 250mW, 2%, 100ppm	01/01/084Y
R17	8.2kΩ, 250mW, 2%, 100ppm	01/01/0921
R18	75Ω, 250mW, 2%, 100ppm	01/01/0263
R19	1.5kΩ, 250mW, 2%, 100ppm	01/01/0697
R20	39Ω, 250mW, 2%, 100ppm	01/01/0182
R21	150Ω, 250mW, 2%, 100ppm	01/01/0387
R22	1.5kΩ, 250mW, 2%, 100ppm	01/01/0697
R23-R25	75Ω, 250mW, 2%, 100ppm	01/01/0263
R26-R29	1kΩ, 250mW, 2%, 100ppm	01/01/0646
R30	NOT FITTED	
R31	75Ω, 250mW, 2%, 100ppm	01/01/0263
R32, R33	47kΩ, 250mW, 2%, 100ppm	01/01/1103
R34, R35	120Ω, 250mW, 2%, 100ppm	01/01/0352
R36, R37	100Ω, 250mW, 2%, 100ppm	01/01/0336
R38	8.2kΩ, 250mW, 2%, 100ppm	01/01/0921
R39	4.7kΩ, 250mW, 2%, 100ppm	01/01/084Y
R40-R42	1kΩ, 250mW, 2%, 100ppm	01/01/0646
R43, R44	2.2kΩ, 250mW, 2%, 100ppm	01/01/1642
R45	10kΩ, 250mW, 2%, 100ppm	01/01/0948
R46	4.7kΩ, 250mW, 2%, 100ppm	01/01/084Y
R47	1.5kΩ, 250mW, 2%, 100ppm	01/01/0697
R48	2.2kΩ, 250mW, 2%, 100ppm	01/01/1642
R49, R50	22kΩ, 250mW, 2%, 100ppm	01/01/1014
R51	1kΩ, 250mW, 2%, 100ppm	01/01/0646
R52	5.1kΩ, 250mW, 2%, 100ppm	01/01/0867
R53, R54	3.3kΩ, 250mW, 2%, 100ppm	01/01/0786
R55	12kΩ. 250mW, 2%, 100ppm	01/01/0964

17413 Component List

RESISTORS (Cont.)

REF.	DESCRIPTION	STOCK CODE
R56, R57	470Ω, 250mW, 2%, 100ppm	01/01/0557
R58	22kΩ, 250mW, 2%, 100ppm	01/01/1014
R59	1kΩ, 250mW, 2%, 100ppm	01/01/0646
R60	10kΩ, 250mW, 2%, 100ppm	01/01/0948
R61	1kΩ, 250mW, 2%, 100ppm	01/01/0646
R62	39Ω, 250mW, 2%, 100ppm	01/01/0182
R63	560Ω, 250mW, 2%, 100ppm	01/01/0581
R64	330Ω, 250mW, 2%, 100ppm	01/01/1723
R65	NOT FITTED	
R66, R67	22kΩ, 250mW, 2%, 100ppm	01/01/1014
R68	1kΩ, 250mW, 2%, 100ppm	01/01/0646
R69	5.1kΩ, 250mW, 2%, 100ppm	01/01/0867
R70, R71	3.3kΩ, 250mW, 2%, 100ppm	01/01/0786
R72	12kΩ, 250mW, 2%, 100ppm	01/01/0964
R73, R74	470Ω, 250mW, 2%, 100ppm	01/01/0557
R75	22kΩ, 250mW, 2%, 100ppm	01/01/1014
R76	1kΩ, 250mW, 2%, 100ppm	01/01/0646
R77	10kΩ, 250mW, 2%, 100ppm	01/01/0948
R78	1kΩ, 250mW, 2%, 100ppm	01/01/0646
R79	47Ω, 250mW, 2%, 100ppm	01/01/0204
R80	330Ω, 250mW, 2%, 100ppm	01/01/1723
R81	1.8kΩ, 250mW, 2%, 100ppm	01/01/070Y
R82	68Ω, 250mW, 2%, 100ppm	01/01/0247
R83	2.2MΩ, 125mW, 5%	01/06/0171
R84, R85	1MΩ, 330mW, 5%, 250ppm	01/01/1332
R86	150kΩ, 250mW, 2%, 100ppm	01/01/1669
R87	5.6kΩ, 250mW, 2%, 100ppm	01/01/0875
R88	100kΩ, 250mW, 2%, 100ppm	01/01/1162
R89	4.7kΩ, 250mW, 2%, 100ppm	01/01/084Y
R90	2.2kΩ, 250mW, 2%, 100ppm	01/01/1642
R91, R92	1kΩ, 250mW, 2%, 100ppm	01/01/0646
R93	2.7kΩ, 250mW, 2%, 100ppm	01/01/0743
R94	10kΩ, 250mW, 2%, 100ppm	01/01/0948

RESISTORS (Cont.)

REF.	DESCRIPTION	STOCK CODE
R95	6.8kΩ, 250mW, 2%, 100ppm	01/01/0905
R96	3.3kΩ, 250mW, 2%, 100ppm	01/01/0786
R97	39Ω, 250mW, 2%, 100ppm	01/01/0182
R98	1kΩ, 250mW, 2%, 100ppm	01/01/0646
R99	120Ω, 250mW, 2%, 100ppm	01/01/0352
R100	39Ω, 250mW, 2%, 100ppm	01/01/0182
R101	1kΩ, 250mW, 2%, 100ppm	01/01/0646
R102	1.5kΩ, 250mW, 2%, 100ppm	01/01/0697
R103	22Ω, 250mW, 2%, 100ppm	01/01/0131
VR1	5kΩ, 50mW. 10%	02/02/0068
VR2	500Ω, 50mW, 10%	02/02/0033
VR3	500Ω, 50mW, 10%	02/05/0021
VR4	1kΩ, 50mW, 10%	02/02/0041
VR5	100Ω, 50mW, 10%	02/02/0017
VR6, VR7	200Ω, 50mW, 10%	02/02/0025
VR8, VR9	1kΩ, 50mW, 10%	02/02/0041
VR10	5kΩ, 50mW, 10%	02/02/0068
VR11	1kΩ, 50mW, 10%	02/02/0641
VR12	5kΩ, 50mW, 10%	02/02/0068
VR13	1kΩ, 50mW, 10%	02/02/0641
VR14	50Ω, 50mW, 20%	02/04/014X
VR15, VR16	10kΩ, 50mW, 10%	02/02/0076
VR17	50Ω, 50mW, 10%	02/04/0018

SEMICONDUCTORS

REF.	DESCRIPTION	STOCK CODE
TR1--TR5	Transistors NPN BC239C	05/01/0446
TR6	Transistor PNP BC309C	05/01/0454
TR7-TR12	Transistors NPN BC239C	

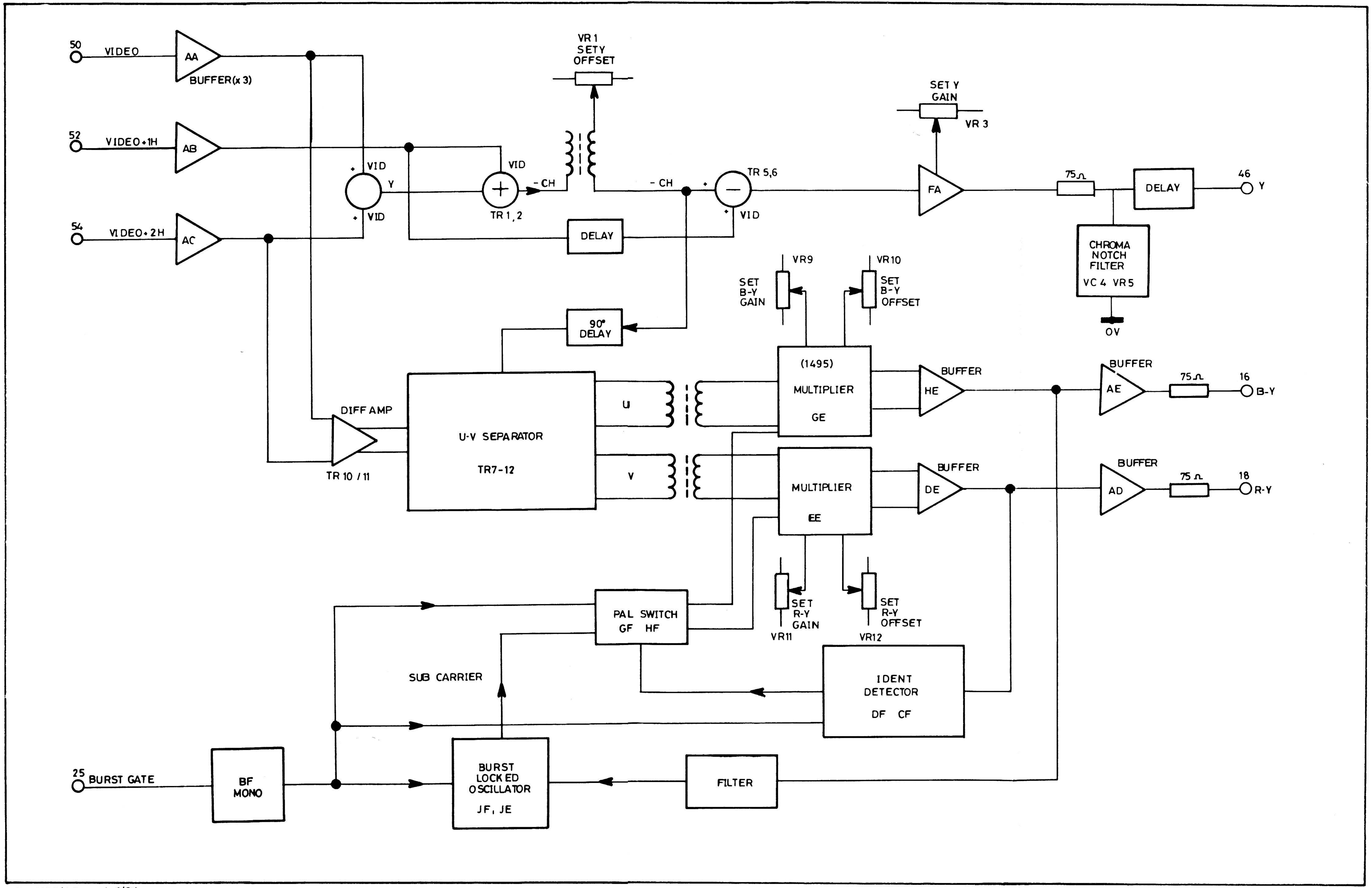
INTEGRATED CIRCUITS

REF.	DESCRIPTION	STOCK CODE
AA-AE	0033CG	04/02/0111
BF	74LS221N	04/01/1589
CF	521N	04/01/2208
DE	3507J	04/02/012X
DF	74LS113N	04/01/5029
EB	Delay Line	30/01/0191
EE	1495L	04/01/1902
EF	74S86N	04/01/0825
FA	0024CH	04/02/0103
GC	Delay Line	
GE	1495L	04/01/1902
GF	74LS221N	04/01/1589
HE	3507J	04/02/012X
HF	74LS221N	04/01/1589
JD	172BP	04/01/2194
JE	4605-5	04/03/1598

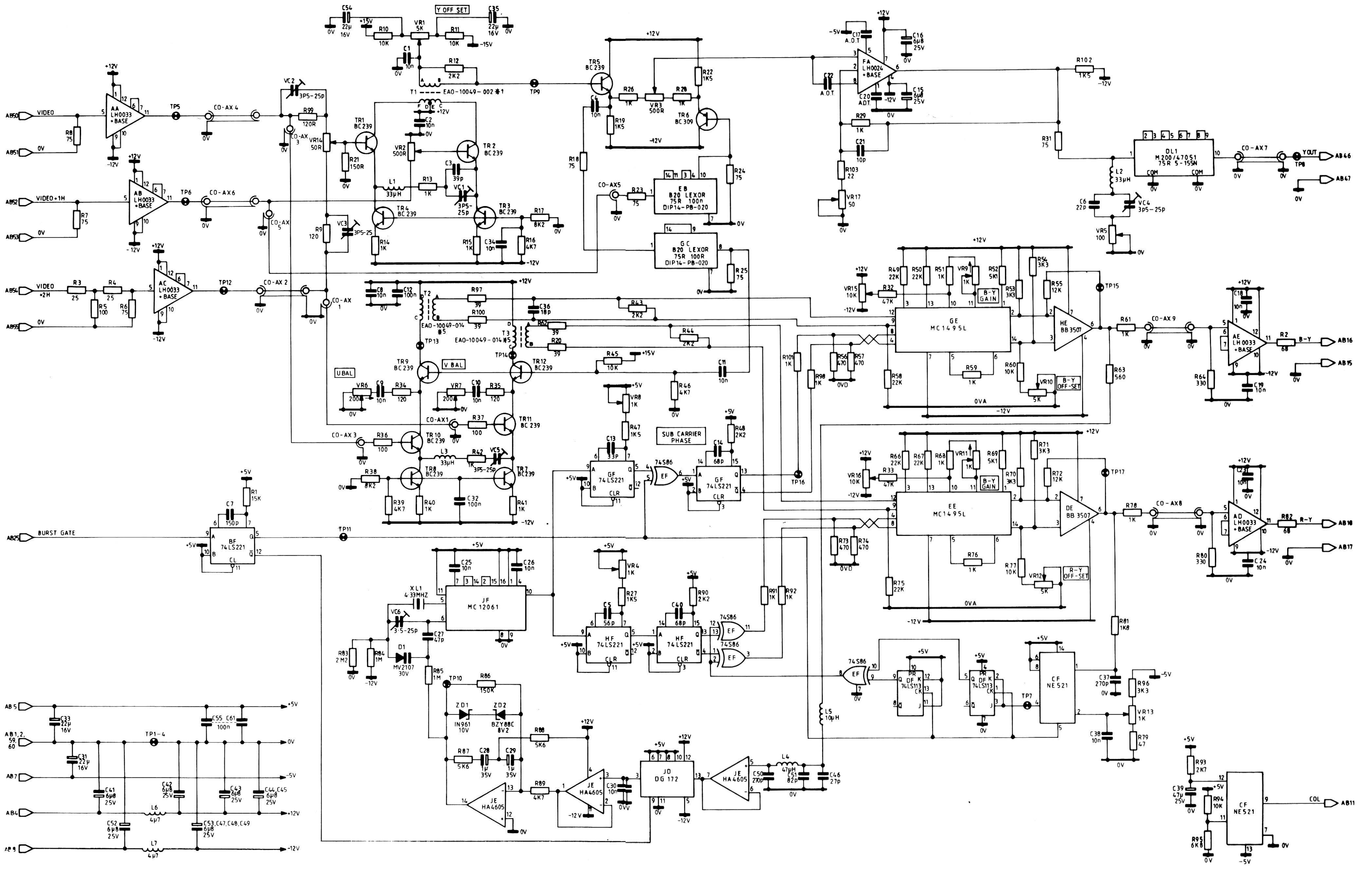
17413 Component List (Cont.)

REF.	DESCRIPTION	STOCK CODE
MISCELLANEOUS		
L1-L3	Inductor 33μH, 250mA, 10%	07/01/0133
L4	Inductor 47μH, 235mA, 10%	07/01/0141
L5	Inductor 10μH, 445mA, 10%	07/01/0079
L6, L7	Inductor 4.7μH, 260mA, 10%	07/01/0052
XL1	Crystal Oscillator 4.433619MHz	28/01/0109

17413 Component List (Cont.)



17413, Figure 1 Chroma Separator Card Block Diagram



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17413, Figure 2 Chroma Separator Card : Circuit Diagram and Component Layout

CHROMA DELAY LINE CARD

17326

1. CIRCUIT DESCRIPTION

Each DSC contains two chroma delay line cards. The card in the lower connector is for NTSC modes, and that in the upper connector is for PAL modes; both are preset to 64µs delay. The delay medium is a glass delay line of the desired length and response.

The video signal is modulated on an R.F. carrier with its sidebands centred within the bandpass of the glass line. After transmission of the modulated carrier through the glass line, the signal is amplified and demodulated to recover the original video input.

The input stage (TR1) is an emitter follower with an input impedance of 75Ω. The input impedance may be made greater than 1kΩ bridging by the removal of R1. A 70nS tapped delay line serves as a vernier delay adjustment and compensates for variances in circuit delays as well as the initial delay tolerance of the glass line. A crystal oscillator (TR5) supplies a stable 27MHz carrier to the modulator (IC1). The modulator frequency pre-emphasis is adjusted by C5 to achieve an essentially flat output to 5MHz. TR2, 3 and 4 form a class B drive amplifier whose operating point is adjusted by R20 for optimum differential gain.

The output of the glass delay line is amplified by a high gain differential video amplifier. The gain of the amplifier is adjusted by R31 to obtain unit gain. After amplification, the signal is demodulated by TR6 and TR7, and is followed by a low pass filter consisting of C18, C19 and L3. The resultant video signal is coupled into the output drive amplifier consisting of TR8, 9 and 10.

The signal is subsequently filtered by a 27MHz trap to remove all traces of the carrier. The trap response is adjusted by C25 for maximum attenuation of the 27MHz carrier. The output impedance of the module is 75Ω.

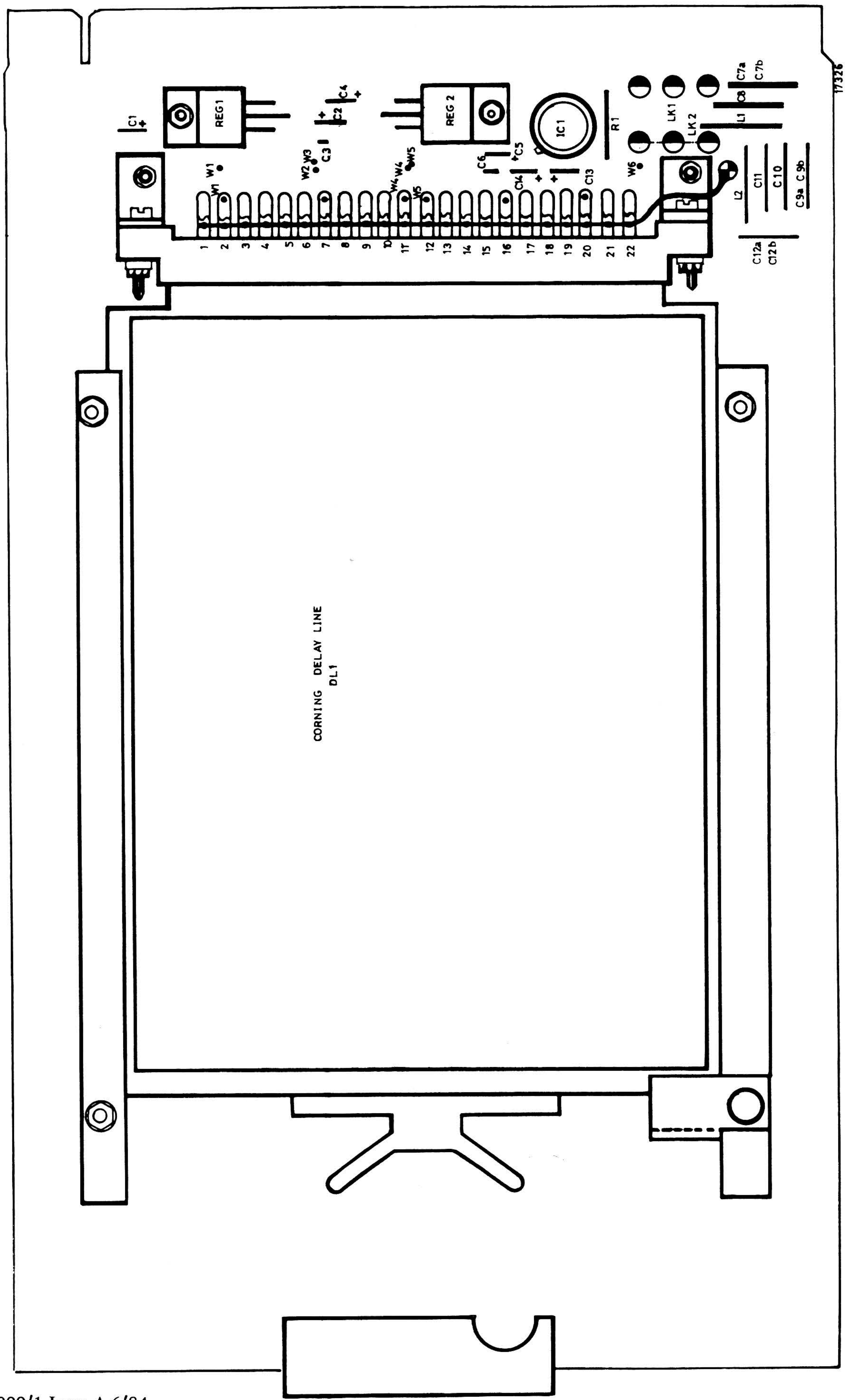
2. ADJUSTMENTS

For access to the Chroma Delay card, loosen the four screws on the rear socket panel and remove the panel. Loosen the knurled screw on the delay line carrier and swing the carrier out. The cards may be removed when the metal tab is swung clear.

Check the input waveforms at TP1 and the oscillator output at TP3. Isolate the trouble to the delay line input circuitry or to the output circuitry by checking the waveforms at points TP5 and TP6 respectively, and then at points TP5 and TP8 respectively. Further isolate the trouble to a particular circuit by normal troubleshooting procedures with the aid of the circuit diagram. Access holes are provided in the component shield for adjustments of C5, R20 and R31.

REF.	DESCRIPTION	STOCK CODE
CAPACITORS		
C1, C2	22µF, 25V, 20%	03/03/0237
C3	100000pF, 50V, +80%-20%	03/06/0233
C4, C5	22µF, 25V, 20%	03/03/0237
C7a	120pF, 50V, 5%	03/04/0232
C7b	47pF, 50V, 5%	03/04/0186
C8	68pF, 50V, 5%	03/04/0208
C9a	330pF, 50V, 5%	03/04/0348
C9b	22pF, 50V, 5%	03/04/0135
C10	33pF, 50V, 5%	03/04/016X
C11	22pF, 50V, 5%	03/04/0135
C12a	220pF, 50V, 5%	03/04/0305
C12b	10pF, 50V, 0.5%	03/04/0097
C13, C14	6.8µF, 25V, 20%	03/03/0148
RESISTORS		
R1	75Ω, 250mW, 2%, 100ppm	01/01/0263
INTEGRATED CIRCUITS		
IC1	0033CG	04/02/0111
MISCELLANEOUS		
L1	1µH, 830mA, 10%	07/01/0028
L2	1.5µH, 600mA, 10%	07/01/281D
REG1	12V	05/04/0035
REG2	12V	05/04/0116

17326 Component List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REG1
C2
C3
C4
W1
W2
W3
W4
W5
REG 2
IC1
C5
C6
C14
C13
R1
W6
LK1
LK2
L1
L2
C7a
C7b
C8
C9a
C9b
C10
C11
C12a
C12b
17326
1
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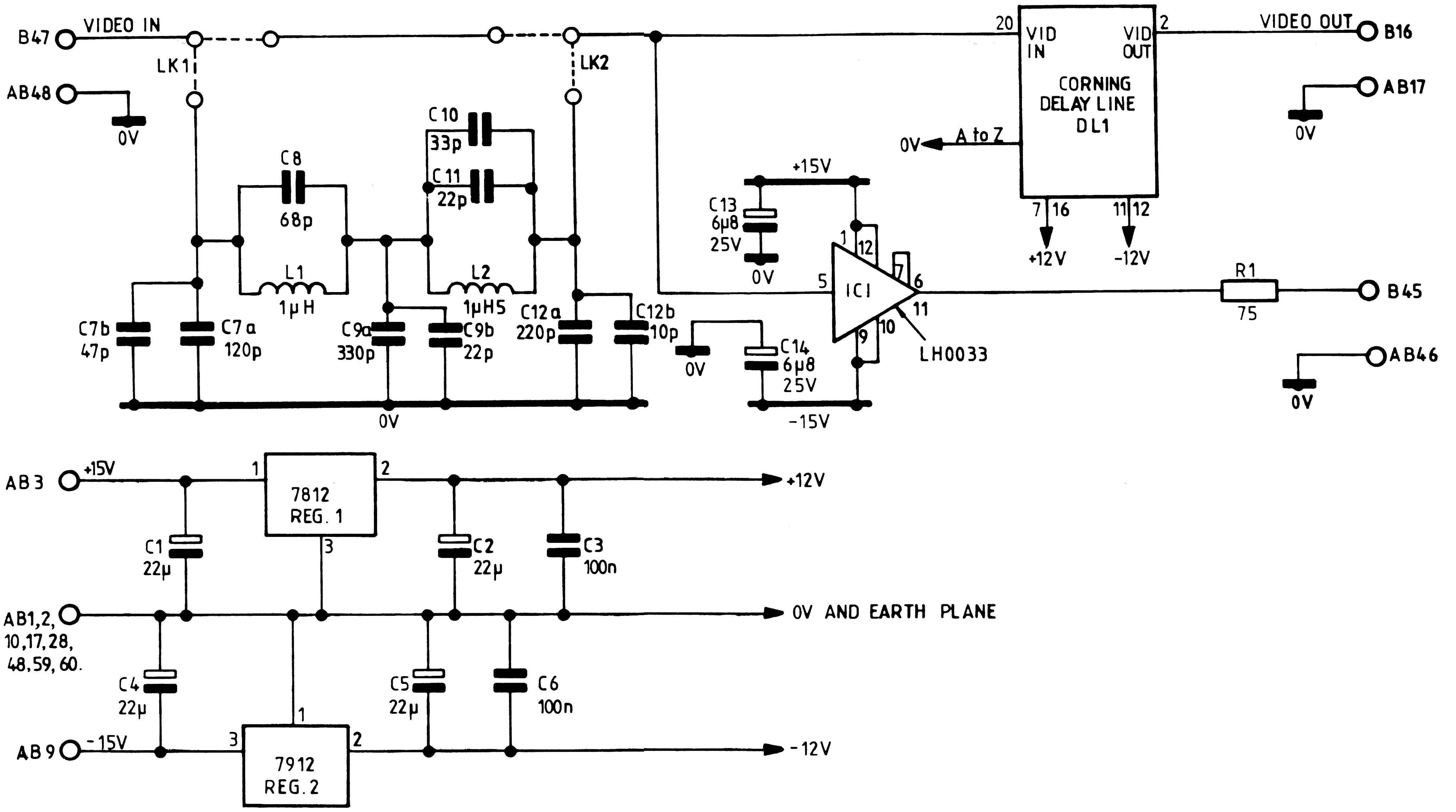
CORNING DELAY LINE
DL1



Issue D 6.8.82

17326, Figure 1 Chroma Delay Line Card : Circuit Diagram and Component Layout

CHROMA SEPARATOR CARD

17441 (NTSC)

1. INTRODUCTION

This card operates closely with the one line delay card and separates the composite video signal into luminance, R-Y and B-Y components which are then digitised by the ADC card.

2. CIRCUIT DESCRIPTION

The Chroma Separator card decodes the composite NTSC video signal into its luminance (Y) and chrominance baseband (R-Y and B-Y) components. It operates in conjunction with two Delay cards type 17462 (ot 17326-105 in some versions) each of which delays the video signal by one television line. The video signal from these Delay cards provides the input for the chroma separator on edge connector pins AB50, AB52 and AB54 delayed by zero, one and two line periods respectively. The cards may be divided into three functional blocks, namely; a luminance separator, a burst-locked oscillator, and a chrominance demodulator, each of which will now be described.

3. LUMINANCE SEPARATION

The three video inputs to the card are first buffered by AA, AB and AC. Then the outer lines are averaged by VR1 and subtracted from the centre line by the combined filter-subtractor circuit TR1-TR4, T1, L1, R12, C70 and VC6.

This results in only subcarrier being present on the secondary of T1, the luminance component being removed by the subtraction and filtering processes. The composite signal from the centre line is then delayed by DL3, to compensate for delays in the filter-subtractor, before being added to 180° phase shifted subcarrier from T1, by TR5 and TR6 to produce pure luminance. The luminance signal is then amplified by TR7-TR10 before being notch filtered by L6, VR6, VC4 and C66 to remove any residual subcarrier components. Delay line DL1 compensates for the time delay difference between the luminance and chrominance channels; but it should be noted that the delay line on the ADC card affects both RGB and encoded chrominance to luminance delay, and should be adjusted first, if necessary, to compensate for any RGB chroma-luma delay.

4. BURST LOCKED OSCILLATOR AND DEMODULATOR

Subcarrier from T1 is fed into the four quadrant multipliers DD and DC together with a subcarrier square wave derived from the VCO. The multiplying action demodulates the R-Y and B-Y components from the subcarrier which are then filtered and buffered before being fed off card to the ADC. The hue control operates by varying the delay of the reference subcarrier fed to the demodulators relative to the burst phase by means of monostable FG(1), whose pulse width it determined by VR13 via current mirror TR11, TR12. A coarse hue control of ±180° is provided by selecting subcarrier from either side of GF pins 1 and 2 by means of SW1. The quadrature of the subcarrier fed to the demodulators is determined by monostable EG(2) while monostables FG(2) and EG(1) restore the reference subcarrier to a square wave.

During the burst gate period, the data selector GG bypasses the hue control to the R-Y demodulator, the output of which is then sampled by CG and C27, buffered and integrated by DG to provide the control volts for the VCO.

5. SET UP PROCEDURE - LUMINANCE CHANNEL

The most likely reason for the chroma separator to malfunction is that the gain and/or frequency response of one of the delay lines will have drifted from its factory setting so that the signals at TP5, TP6 and TP7 are not longer identical amplitude. This must be checked using a multiburst input signal before any adjustments are made to the chroma separator. After this has been done, VR1 should be set to its mid-position, then, with multiburst as the input and an oscilloscope probe attached to the base of TR5, VR2 should be adjusted to minimise the amplitude of the multiburst visible on the oscilloscope. If, at any point in the set-up procedure, the correct signal is not present, check that VR15 (output d.c. level) has not been set so as to clip the signal at the supply units.

Change the input signal to colour bars and connect an oscilloscope or vectorscope to TP11, then adjust VC6 and VR3 for minimum subcarrier amplitude. To complete the setting up of the luminance channel, set VC4 and VR6 for minimum residual subcarrier at the output of the card; the black level to 0V with VR15, and the output signal to 1V p-p with VR4.

6. SET UP PROCEDURE - CHROMINANCE CHANNEL

With colour bars as an input and an oscilloscope probe on TP13, adjust VR7 to balance the modulators, and VR9 to set the d.c. level to 0V. Repeat this procedure for TP16, VR10 and VR12. Attach the probe to TP19 and adjust VC5 to bring the control volts to 0V.

Turn off B-Y on the colour bar generator, and adjust the hue controls (VR13 and SW1) to zero the signal at TP14. Then turn B-Y on and R-Y off, and by adjusting VR14 only, zero the signal at TP17. Finally set VR8 and VR11 to give a 4V p-p signal at TP14 and TP17 with 75% bars as input.

REF.	DESCRIPTION	STOCK CODE
CAPACITORS		
C1-C6	6.8µF, 25V, 20%	03/03/0148
C7	10000pF, 100V, +80%-20%	03/06/0101
C8, C9	100000pF, 50V, +80%-20%	03/06/0233
C10	6.8µF,25V, 20%	03/03/0148
C11	270pF, 100V, 10%	03/06/0349
C12	39pF, 100V, 10%	03/06/0039
C13-C16	10000pF, 100V, +80%-20%	03/06/0101
C17-C19	NOT FITTED	
C20, C21	1µF, 35V, 20%	03/03/004Y
C22, C23	100000pF, 50V, +80%-20%	03/06/0233
C24	120pF, 100V, 10%	03/01/0414
C25	15µF, 25V, 20%	03/03/0415
C26	39pF, 100V, 10%	03/06/0039
C27	10000pF, 100V, +80%-20%	03/06/0101
C28-C30	NOT FITTED	
C31	68pF, 100V, 10%	03/06/0497
C32-C37	6.8µF, 25V, 20%	03/03/0148
C38	100000pF, 50V, +80%-20%	03/06/0101
C39-C60	10000pF, 100V, 380%-20%	03/06/0101
C61-C63	100000pF, 50V, +80%-20%	03/06/0233
C64, C65	6.8µF, 25V, 20%	03/03/0148
C66	100pF, 100V, 10%	03/06/0306
C67	270pF, 100V, 10%	03/06/0349
C68	22000pF, 100V, 5%	03/00/0843
C69	22pF, 100V, 5%	03/06/0667
C70	18pF, 100V, 5%	03/06/0411
C71, C72	10000pF, 100V, +80%-20%	03/06/0101
VC1	NOT FITTED	
VC2, VC3	160V, -10%+70%	03/07/0077
VC4	250V, -10%+70%	03/07/0115
VC5	NOT FITTED	
VC6	50V	03/07/0212
VC7	250V, -10%+50%	03/07/0069
RESISTORS		
R1, R2	75Ω, 250mW, 2%, 100ppm	01/01/0263
R3, R4	25Ω, 125mW, 0.1%, 50ppm	01/03/0035
R5	100Ω, 250mW, 2%, 100ppm	01/01/0336
R6	75Ω, 250mW, 2%, 100ppm	01/01/0263
R7	15kΩ, 250mW, 2%, 100ppm	01/01/0972
R8	120Ω, 250mW, 2%, 100ppm	01/01/0352
R9	150Ω, 250mW, 2%, 100ppm	01/01/0387
R10	120Ω, 250mW, 2%, 100ppm	01/01/0352
RESISTORS (Cont.)		
R11	2.2kΩ, 250mW, 2%, 100ppm	01/01/1642
R12-R14	1kΩ, 250mW, 2%, 100ppm	01/01/0646
R15	4.7kΩ, 250mW, 2%, 100ppm	01/01/084Y
R16	8.2kΩ, 250mW, 2%, 100ppm	01/01/0921
R17	100Ω, 250mW, 2%, 100ppm	01/01/0336
R18	1kΩ, 250mW, 2%, 100ppm	01/01/0646
R19	200Ω, 250mW, 2%, 100ppm	01/01/0425
R20	1.1kΩ, 250mW, 2%, 100ppm	01/01/0654
R21	100Ω, 250mW, 2%, 100ppm	01/01/0336
R22, R23	10kΩ, 250mW, 2%, 100ppm	01/01/0948
R24	NOT FITTED	
R25	1kΩ, 250mW, 2%, 100ppm	01/01/0646
R26	22Ω, 250mW, 2%, 100ppm	01/01/0131
R27, R28	1kΩ, 250mW, 2%, 100ppm	01/01/0646
R29	1.2kΩ, 250mW, 2%, 100ppm	01/01/0662
R30	1kΩ, 250mW, 2%, 100ppm	01/01/0646
R31	270Ω, 250mW, 2%, 100ppm	01/01/0476
R32	75Ω, 250mW, 2%, 100ppm	01/01/0263
R33	56kΩ, 250mW, 2%, 100ppm	01/01/112X
R34, R35	22kΩ, 250mW, 2%, 100ppm	01/01/1014
R36	270Ω, 250mW, 2%, 100ppm	01/01/0476
R37	5.1kΩ, 250mW, 2%, 100ppm	01/01/0867
R38, R39	3.3kΩ, 250mW, 2%, 100ppm	01/01/0786
R40	12kΩ, 250mW, 2%, 100ppm	01/01/0964
R41, R42	75Ω, 250mW, 2%, 100ppm	01/01/0263
R43	68Ω, 250mW, 2%, 100ppm	01/01/0247
R44, R45	22kΩ, 250mW, 2%, 100ppm	01/01/1041
R46, R47	470Ω, 250mW, 2%, 100ppm	01/01/0557
R48	22kΩ, 250mW, 2%, 100ppm	01/01/1014
R49	NOT FITTED	
R50	10kΩ, 250mW, 2%, 100ppm	01/01/0948
R51	NOT FITTED	
R52	5.1kΩ, 250mW, 2%, 100ppm	01/01/0867

17441 Component List

RESISTORS (Cont.)

REF.	DESCRIPTION	STOCK CODE
R53	56kΩ, 250mW, 2%, 100ppm	01/01/112X
R54, R55	22kΩ, 250mW, 2%, 100ppm	01/01/1014
R56	270Ω, 250mW, 2%, 100ppm	01/01/0476
R57	5.1kΩ, 250mW, 2%, 100ppm	01/01/0867
R58, R59	3.3kΩ, 250mW, 2%, 100ppm	01/01/0786
R60	12kΩ, 250mW, 2%, 100ppm	01/01/0964
R61, R62	75Ω, 250mW, 2%, 100ppm	01/01/0263
R63	68Ω, 250mW, 2%, 100ppm	01/01/0247
R64, R65	470Ω, 250mW, 2%, 100ppm	01/01/0557
R66	NOT FITTED	
R67	10kΩ, 250mW, 2%, 100ppm	01/01/0948
R68, R69	22kΩ, 250mW, 2%, 100ppm	01/01/1014
R70	NOT FITTED	
R71	1kΩ, 250mW, 2%, 100ppm	01/01/0646
R72	680Ω, 250mW, 2%, 100ppm	01/01/059X
R73	10kΩ, 250mW, 2%, 100ppm	01/01/0948
R74	2kΩ, 250mW, 2%, 100ppm	01/01/0719
R75	5.1kΩ, 250mW, 2%, 100ppm	01/01/0867
R76	1.8kΩ, 250mW, 2%, 100ppm	01/01/1669
R77	NOT FITTED	
R78	150kΩ, 250mW, 2%, 100ppm	01/01/1669
R79	5.6kΩ, 250mW, 2%, 100ppm	01/01/0875
R80	NOT FITTED	
R81	4.7kΩ, 250mW, 2%, 100ppm	01/01/084Y
R82	680Ω, 250mW, 2%, 100ppm	01/01/059X
R83	100Ω, 250mW, 2%, 100ppm	01/01/0336
R84	1.2kΩ, 250mW, 2%, 100ppm	01/01/0263
R85	75Ω, 250mW, 2%, 100ppm	01/01/0263
R86	NOT FITTED	
R87-R89	100kΩ, 250mW, 2%, 100ppm	
R90	2.2kΩ, 250mW, 2%, 100ppm	01/01/1642
R91	1kΩ, 250mW, 2%, 100ppm	01/01/0646
R92-R94	100kΩ, 250mW, 2%, 100ppm	
R95	120kΩ, 250mW, 2%, 100ppm	01/01/117Y
R96	22kΩ, 250mW, 2%, 100ppm	01/01/1014
R97	75Ω, 250mW, 2%, 100ppm	01/01/0263
R98	10kΩ, 250mW, 2%, 100ppm	01/01/0948

RESISTORS (Cont.)

REF.	DESCRIPTION	STOCK CODE
R99	47kΩ, 250mW, 2%, 100ppm	01/01/1103
R100	100kΩ, 250mW, 2%, 100ppm	
R101	47kΩ, 250mW, 2%, 100ppm	01/01/1103
VR1	50Ω, 50mW, 20%	02/04/014X
VR2	500Ω, 50mW, 10%	02/02/0033
VR3	2kΩ, 50mW, 10%	02/02/005X
VR4	100Ω, 50mW, 10%	02/02/0017
VR5	NOT FITTED	
VR6	100Ω, 50mW, 10%	02/02/0017
VR7	10kΩ, 50mW, 10%	02/02/0076
VR8	1kΩ, 50mW, 10%	02/02/0041
VR9	5kΩ, 50mW, 10%	02/02/0068
VR10	10kΩ, 50mW, 10%	02/02/0076
VR11	1kΩ, 50mW, 10%	02/02/0041
VR12	5kΩ, 50mW, 10%	02/02/0068
VR13	5kΩ, 50mW, 10%	02/03/0047
VR14	1kΩ, 50mW, 10%	02/02/0041
VR15	NOT FITTED	
VR16	200kΩ, 50mW, 10%	02/02/0149

SEMICONDUCTORS

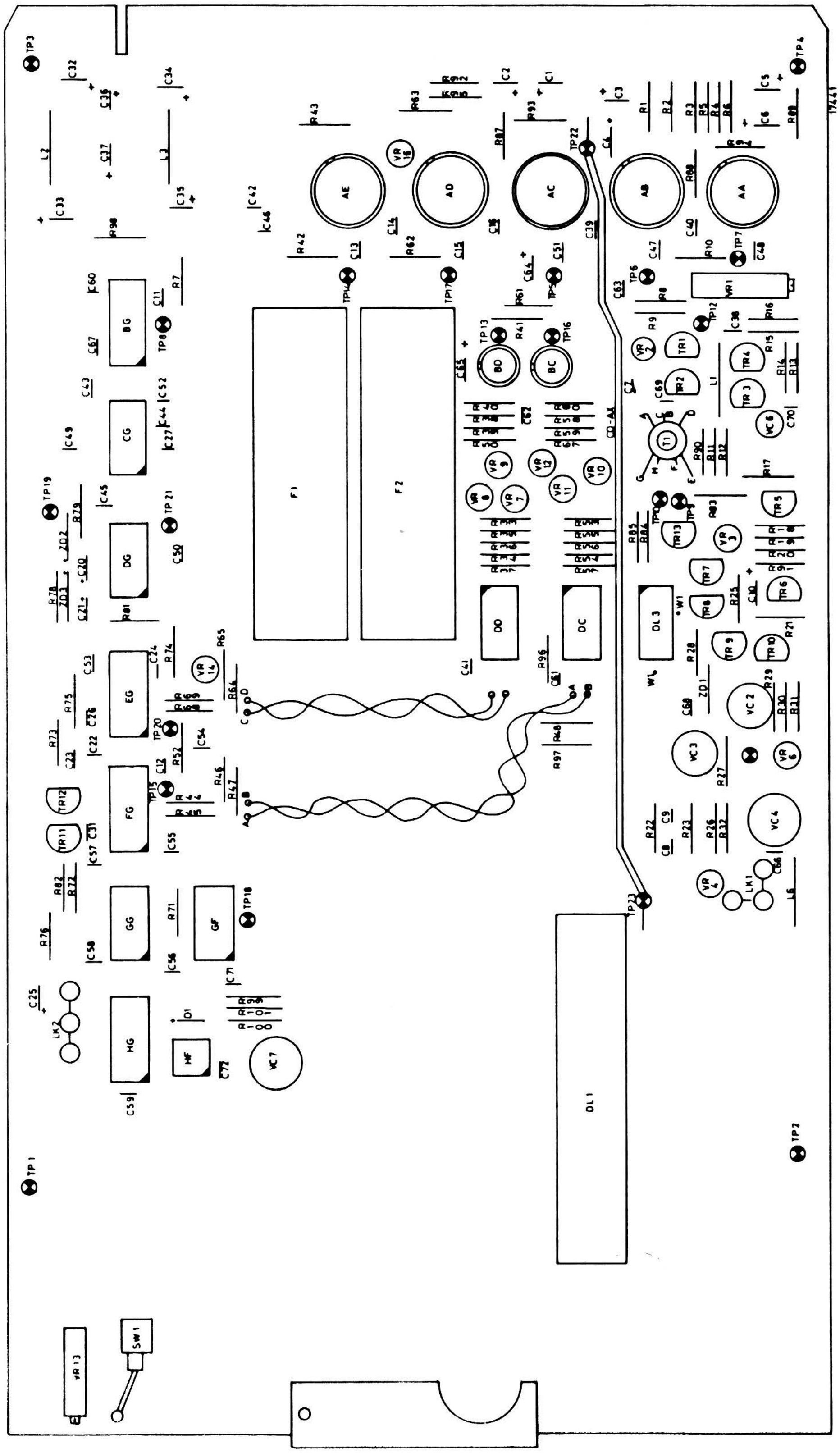
REF.	DESCRIPTION	STOCK CODE
D1	NOT FITTED	
D2	Diode 30V, 350mW	06/05/0018
ZD1	Zener Diode 4.7V, 500mW	06/02/0186
ZD2	Zener Diode 10V, 400mW	06/02/0267
ZD3	Zener Diode 8.2V, 500mW	06/02/0135

INTEGRATED CIRCUITS

REF.	DESCRIPTION	STOCK CODE
AA-AE	0033CG	04/02/0111
BC, BD	3507J	04/02/012X
BG	74221N	04/01/157Y
CG	172BP	04/01/2194
DC, DD	1495L	04/01/1902
DG	74S04N	04/01/0167
EG, FG	74221N	04/01/157Y
GF	74S04N	04/01/0167
GG	74LS51N	04/01/3263
HG	74LS161N	04/01/1287
HF	Crystal Osc. 14.318MHz	28/02/0236

MISCELLANEOUS

REF.	DESCRIPTION	STOCK CODE
L1-L3	Inductor 47μH, 235mA, 10%	07/01/0141
L4, L5	NOT FITTED	
L6	18μH, 280mA, 10%	07/01/0117
SW1	Toggle Switch	26/02/0166
XL1	NOT FITTED	
DL1	Delay Line	30/01/0078
DL2	NOT FITTED	
DL3	Delay Line	30/01/0175


17441
TP1
TP2
TP3
TP4
TP6
TP7
TP8
TP12
TP13
TP14
TP15
TP16
TP17
TP18
TP19
TP20
TP21
TP22
TP23
AA
AB
AC
AD
AE
BC
BD
BG
CG
DG
EG
FG
GG
GF
HG
HF
F1
F2
DD
DC
DL1
DL3
VC2
VC3
VC4
VC6
VC7
T1
L1
L2
L3
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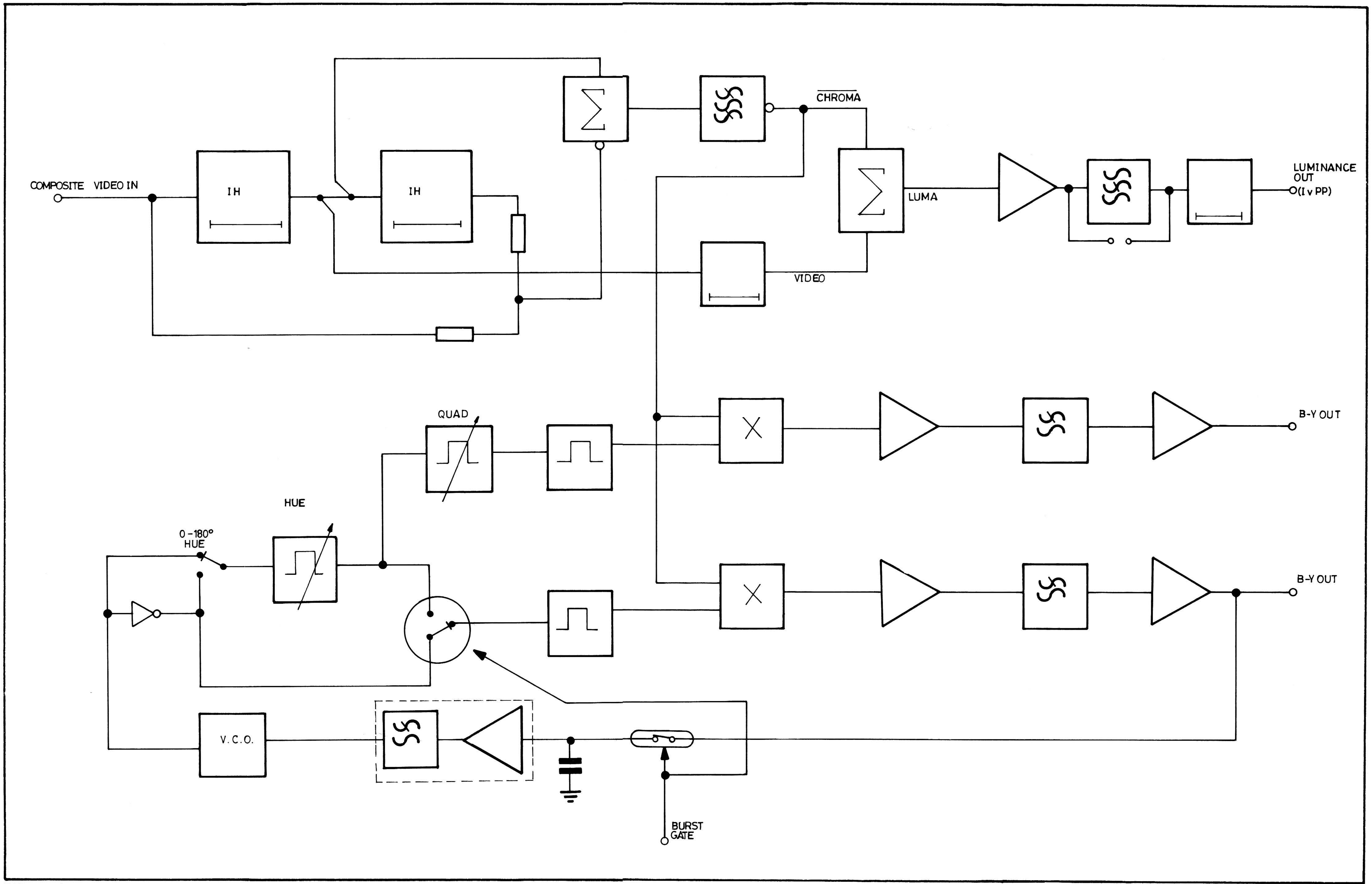
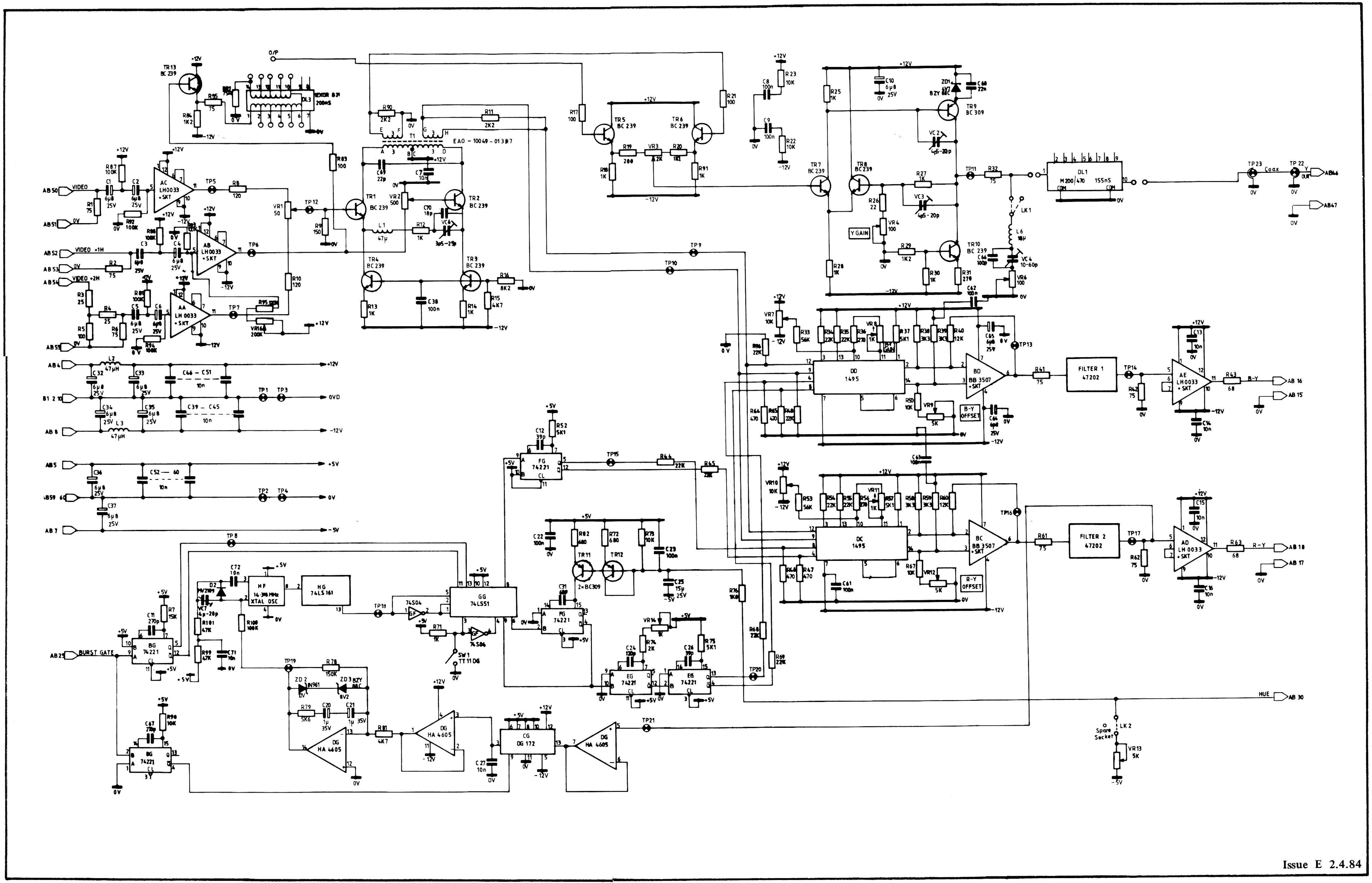
B
C
D



17441, Figure 1 Chroma Separator Card Block Diagram



Issue E 2.4.84

17441, Figure 2 Chroma Separator Card : Circuit Diagram and Component Layout

TABLET CONTROLLER (ID20) INTERFACE CARD

17479

1. INTRODUCTION

The 17479 Interface card is mounted inside the Tablet Controller and has two 25-way D-type connectors which are accessible at the rear of the controller. The plug is for the ARTIST cable to the Paintbox and the socket is for the keyboard and joystick. Internally there are four interconnecting cables to the Tablet Controller.

(a) 50-way flat cable. This provides +5V and 0V logic supplies and receives parallel position data from the tablet electronics.

(b) 34-way connector with only two wires providing:

+12V for the pressure circuitry
−12V for the keyboard.

(c) 5-way bergstick connector that goes to the pen.

(d) 16-pin DIL socket which connects to the front panel LED display. This was not fitted on early versions.

2. CIRCUIT DESCRIPTION

This card uses a 6803 microprocessor, running software in EPROM BA, to gather data from the tablet electronics, the keyboard and the pen circuitry. It assembles a packet of information which is sent serially to the Paintbox. The serial link is RS422 compatible from differential driver AB.

Data from the tablet is read via tristate buffers DG, DD, DF and DE. These buffers are memory mapped, the addresses being decoded by LS138's BB and BC. BB generates write strobes. BC generates read strobes. The processor address bus A/D 0 - 7 carries multiplexed addresses and data. BD separates addresses using address strobe AS (pin 39 of 6803). The microprocessor has an 8-bit parallel port on chip and this is used to monitor signals DR, PROX, Z-AXIS from the tablet. PROX is active when the pen is in proximity and DR then strobes low about once every 10μs indicating that parallel data from the tablet is ready. Z-AXIS directly reads the switch on standard Summagraphics pens (non-pressure sensitive). The processor also reads the DIL switches via its parallel port. Switch 2 selects NTSC or PAL scaling. The parallel data from the tablet is scaled appropriately and encoded for serial transmission.

A strobe from the keyboard, when a key is pressed latches the keyboard data in BF and sets AD high. This signals the processor to read the data and when it does so AD is cleared. BG is connected to the joystick switches which when active pull the inputs to BG low. Latch CF is used to drive LEDs on the front panel or on the keyboard.

The pressure sensitive pen contains a transducer which converts pressure into a voltage between pin 2 of socket 4 and ground. Power (7.5V) is supplied via pin 1. DB is a buffer for the high impedance output of the pen. TP1 sits at about 2V and maximum pressure only causes about 50mV change at this point. Amplifier DC has a gain of 180 but with an offset summed into pin 2. This is from Digital to Analogue convertor CA. The DAC is driven by the microprocessor via latch CB in order to provide auto calibration of the pen and minimise drift. The offset is such that when the pen is out of proximity (no pressure) TP2 sits at 1V. Full pen pressure will then take TP2 up to +5V. This voltage is digitised by ADC CC. Zener ZD1 prevents the maximum input voltage of the ADC being exceeded. If the processor cannot make TP2 1V with no pressure then it assumes that a non-pressure sensitive pen is fitted and looks for a Z-AXIS switch. This allows the standard summagraphics pen to be used but with full pressure only.

Pens are fitted at the factory with a trimming resistor in their DIN plug to reduce the spread of characteristics between different pens. No adjustments are necessary on the interface.

Note: DPB 7000 Pens from 10/4/83

These pens have modified ground wiring to improve noise immunity. The proximity coil ground is now isolated from the pressure sensor ground.

On some tablet controllers the yellow wire between the pen socket and the ID20 17479 Interface card has been cut at the 5 pin plug going to the Interface card. This wire is the transducer ground and must be connected for this modified pen to work. If not connected the pen will give proximity and cursor but not pressure.

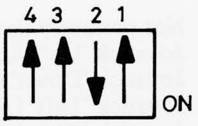
3. SWITCH POSITIONS

(a) ID20 Interface card

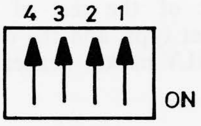
	ON	OFF
1	RESET	NORMAL
2	PAL	NTSC
3	ASCII	BIN
4	MONITOR	NORMAL

Normal Settings

PAL

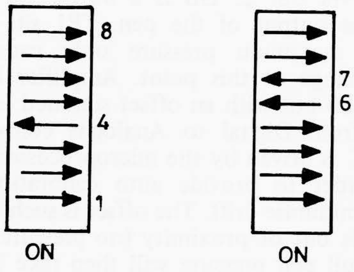


NTSC



(b) ID20 Mother card

Normal Settings



Switch 1 Switch 2

4. DIL SWITCH FUNCTIONS

Switch 1	OFF	Run
	ON	Reset
Switch 2	OFF	NTSC scaling
	ON	PAL scaling
Switch 3	OFF	Selects binary output mode on serial line (normal)
	ON	Selects ASCII output mode, for debugging use. In this mode, all keyboard, status and coordinate values are output in hex
Switch 4	OFF	Selects power-up into main program
	ON	Selects power-up into monitor, rather than main program

5. SERIAL LINE PROTOCOL

The data transmitted down the serial line is split into packets. A packet has the following format.

Byte 1 - Packer Header

MS							LS Bit
7	6	5	4	3	2	1	0

Bits 7 = 1	indicates start of packet.
Bits 6 and 5	Packet type bits
	00 (*00) - Coordinate packet 01 (*20) - Keyboard character packet 10 (*40) - 'Out of Proximity' packet 11 (*60) - 'Special' packet
Bit 4	Not presently used
Bit 3	Joystick 'Up' (Active high)
Bit 2	Joystick 'Down' (Active high)
Bit 1	Joystick 'Left' (Active high)
Bit 0	Joystick 'Right' (Active high)

The format of the rest of the packet depends on the packet type, and the only common features are that ONLY packet header bytes are allowed to have the MS bit set, and that the last byte of every packet sent is a checksum of all previous bytes, including the packet header, obtained by XOR'ing the bytes together. The top bit of the checksum is always zero, and should be ignored.

Coordinate packets:- 6 data bytes transmitted.

Byte 2:	X coord high bits (bits 7-13 of 14 bit value)
Byte 3:	X coord low bits (bits 0-6 of 14 bit value)
Byte 4:	Y coord high bits (bits 7-13 of 14 bit value)
Byte 5:	Y coord low bits (bits 0-6 of 14 bit value)
Byte 6:	Pen pressure (0-127) with 127 = full pressure
Byte 7:	Checksum

Keyboard character packets:- 2 data bytes transmitted.

Byte 2:	Character received from keyboard
Byte 3:	Checksum

Out of proximity packets:- 1 data byte transmitted

Byte 2: Checksum

Special packets:- 2 data bytes transmitted

Byte 2: Special packet type:-
0 : Power up for PAL system
1 : Power up for NTSC system

Byte 3: Checksum

X Y Scaling

Tablet =0.1mm per bit
adjust for A4 (297mm x 210mm)

NTSC

Aspect ratio = 0.85
300mm = 759 x 8
X = X x 2
Y = Y x 1.700 = Y x (2 - 77/256)

PAL

Aspect ratio = 1.11
300mm = 701 x 8
X = X x 1.847 = X x (2 - 39/256)
Y = Y x 2.050 = Y x (2 + 13/256)

6. KEYBOARD AND ROTATE SWITCH CONNECTOR DETAILS

The keyboard is connected to the ID20 Interface card via a 25-way male D-type connector. The rotate switch is wired with a separate cable into this connector.

Inside the keyboard the cable has a 16-pin DIL connector to the circuit board. This must be orientated correctly. The socket has an angle on the corner at pin 1 and the plug has a notch at the end with pin 1.

The connections are as follows:

25-Way	16 Pin DIL
1	12
2	13
3	10
4	1
5	6
6	5
7	7
10	2
13	5 (−12V)
14	Rotate switch Y2
15	Rotate switch Y1
16	Rotate switch X2
17	Rotate switch X1
23	1 (+5V)
25	8 and Rotate switch screen (0V)

IMPROVED KEYBOARD

From October 1983 an improved keyboard (Alphanumeric AKL 81-042) will be available for handling text as part of the typography package. This keyboard has two D-type 25-way connectors on the case which are connected pin for pin. A separate cable (D-type male to female) connects the keyboard to the tablet controller. The rotate switch also has a D-type connector and plugs into the keyboard, directly into the tablet controller or onto the keyboard cable, if it is wished to dispense with the keyboard.

Old and new keyboards are directly interchangeable but the new keyboard provides additional facilities. Inside the new keyboard the D-types are wired to a 16 pin I.D. molex connector which plugs into the keyboard pcb. The pinning is as follows:-

Function	25-way D-types	16-way I.D.
D0	1	2
D1	2	4
D2	3	6
D3	4	8
D4	5	10
D5	6	12
D6	7	14
D7	8	16
Strobe	10	3
−12V	13	––
Rotate Switch Y2	14	––
Rotate Switch Y1	15	––
Rotate Switch X2	16	––
Rotate Switch X1	17	––
+5V	23	9
0V	25	15
Rotate Switch Common	16-way Molex	

CAPACITORS

REF.	DESCRIPTION	STOCK CODE
C1, C2	39pF, 100V, 10%	03/06/0039
C3, C4	22μF, 16V, 20%	03/03/0253
C5, C6	22μF, 25V, 20%	03/03/0237
C7	22μF, 16V, 20%	
C8	6.8μF, 16V, 20%	03/03/013X
C9	100000pF, 50V,	03/06/0233
C10	NOT FITTED	
C11, C12	100000pF, 50V, +80%-20%	03/06/0233
C13	10000pF, 100V, +80%-20%	03/06/0101
C14-C37	100000pF, 50V, +80%-20%	03/06/0233
C38-C40	NOT FITTED	
C41	1μF, 35V, 20%	03/03/004Y

RESISTORS

REF.	DESCRIPTION	STOCK CODE
R1-R3	10kΩ, 250mW, 2%, 100ppm	01/01/0948
R4	10kΩ x 4, 125mW, 5%, 300ppm	01/08/1128
R5	180kΩ, 250mW, 2%, 100ppm	01/01/120Y
R6, R7	NOT FITTED	
R8	1kΩ, 250mW, 2%, 100ppm	01/01/0646
R9, R10	NOT FITTED	
R11	1.5kΩ, 250mW, 2%, 100ppm	01/01/0697
R12	22kΩ, 250mW, 2%, 100ppm	01/01/1014
R13	330Ω, 250mW, 2%, 100ppm	01/01/1723
R14	NOT FITTED	
R15	10kΩ, 250mW, 2%, 100ppm	01/01/0948
R16, R17	10kΩ, 250mW, 1%, 50ppm	01/01/2207
R18	1kΩ x 8, 125mW, 5%, 300ppm	01/08/0539

RESISTORS (Cont.)

REF.	DESCRIPTION	STOCK CODE
R19	200Ω, 250mW, 2%, 100ppm	01/01/0425
R20-R23	NOT FITTED	
R24-R31	300Ω, 250mW, 2%, 100ppm	01/01/1723
R32	11kΩ, 250mW, 2%, 100ppm	01/01/0956
R33	3.6kΩ, 250mW, 2%, 100ppm	01/01/0794
R34	560Ω, 250mW, 2%, 100ppm	01/01/0581
VR1	NOT FITTED	

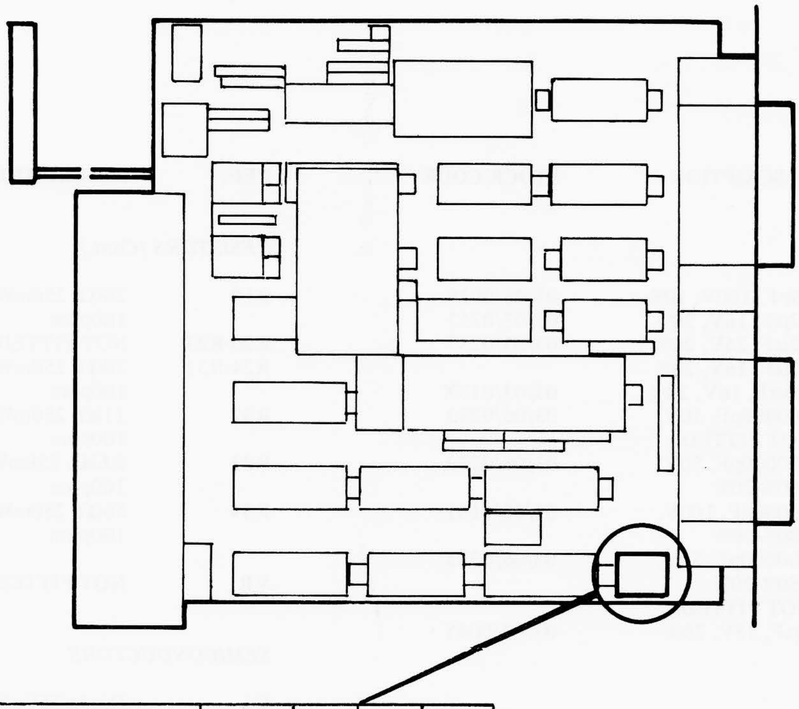
SEMICONDUCTORS

REF.	DESCRIPTION	STOCK CODE
D1	Diode 75V, 500M	06/01/0083
D2	Zener Diode 5.1V, 500mW	06/02/0194
D3	Zener Diode 7.5V, 500mW	06/02/024Y
D4	Zener Diode 10V, 400mW	06/02/0267

INTEGRATED CIRCUITS

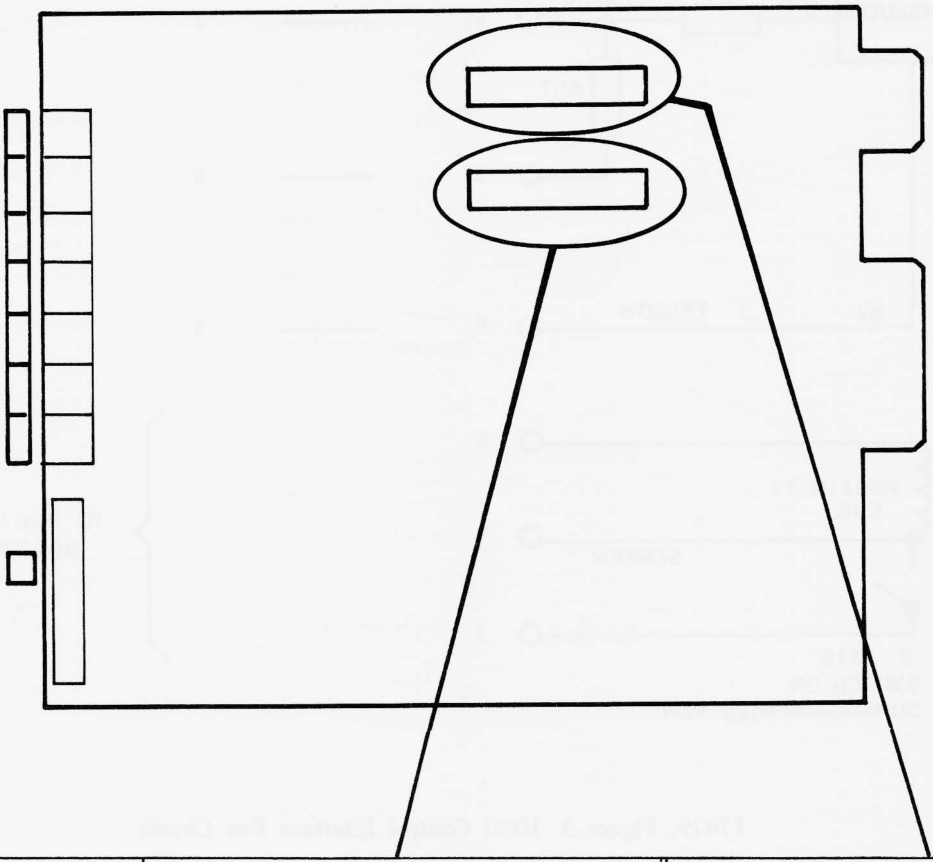
REF.	DESCRIPTION	STOCK CODE
AA	26LS32PC	04/01/4413
AB	26LS31PC	04/01/4405
AC	74LS00N	04/01/006X
AD	74LS74N	04/01/0728
AE	6803L	04/03/3469
AG	Dil Switch	26/05/003Y
BA	2716J-8	04/03/063X
BB, BC	74LS138N	04/01/109Y
BD	74LS373N	04/01/3921
BF	74LS374N	04/01/3328
BG	74LS240N	04/01/2879
CA	08AQ	04/03/0788
CB	74LS374N	04/01/3328
CC	MK5168	29/01/0757
CF	74LS374N	04/01/3328
DB, DC	741CN	04/01/250X
DD-DG	74LS244N	04/01/2828

17479 Component List



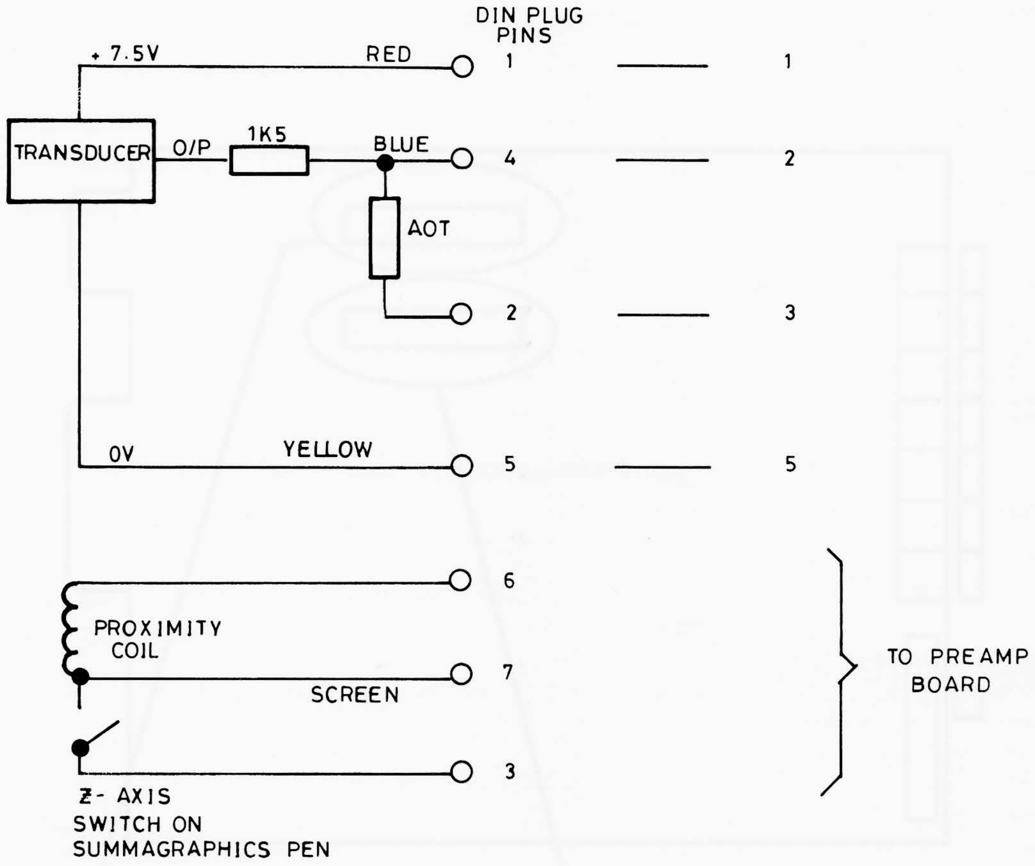
	1	2	3	4
RESET	ON			
7000		OFF		
7001		ON		
BINARY OUTPUT (NORMAL)			OFF	
ASCII (ENGINEERING)			ON	
MONITOR ON SWITCH ON				ON
NORMAL OPERATION				OFF
STANDARD CONFIGURATION				
7000	OFF	OFF	OFF	OFF
7001	OFF	ON	OFF	OFF

17479, Figure 1 ID20 Control Interface Switch Configurations

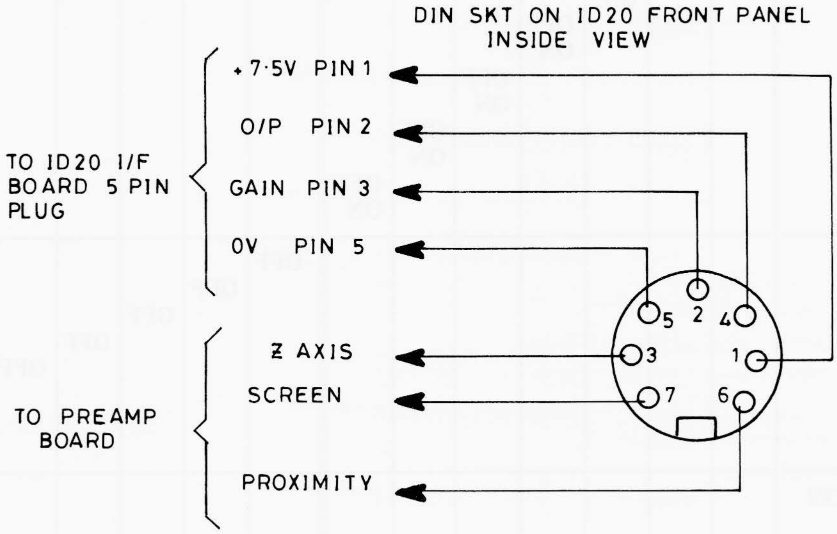


	1	2	3	4	5	6	7	8	1	2	3	4	5	6	7	8
Z AXIS	ON															
FLAG 3		ON														
FLAG 2			ON													
FLAG 1				ON												
NORMAL DIGITISER					OFF											
SELF TEST					ON											
BCD						OFF										
BINARY						ON										
ENGLISH							OFF									
METRIC							ON									
BCD NORMALISED								OFF								
BCD NOT NORMALISED								ON								
Y WEIGHTING 1									OFF							
Y WIEGHTING 2										OFF						
Y WEIGHTING 4											OFF					
X WEIGHTING 1												OFF				
X WEIGHTING 2													OFF			
X WEIGHTING 4														OFF		
X WEIGHTING 8															OFF	
X WEIGHTING 16																OFF
STANDARD CONFIGURATION	OFF	OFF	OFF	OFF	OFF	ON	ON	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF

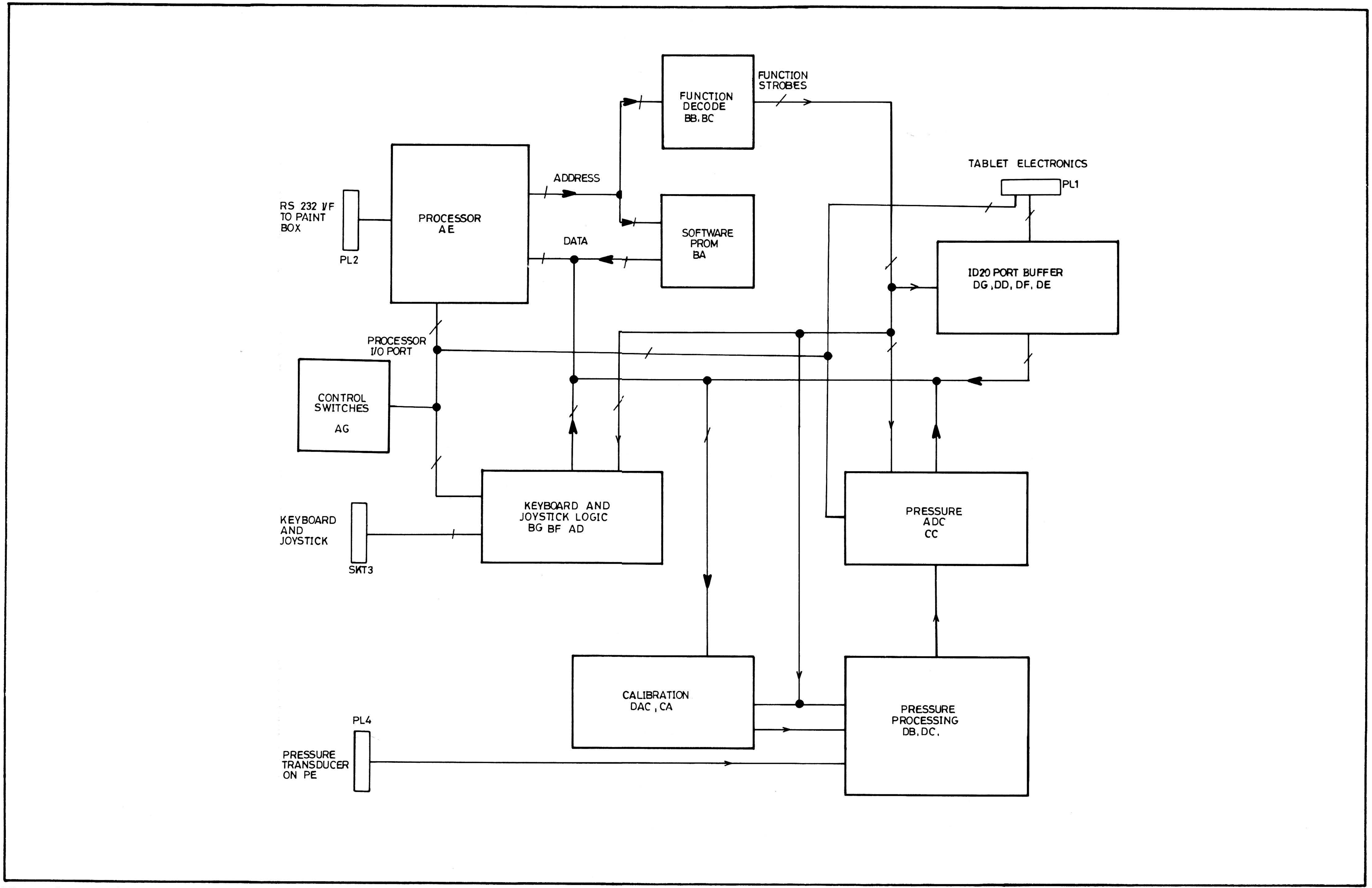
17479, Figure 2 ID20 Control Interface Main Logic Board Switch Configurations



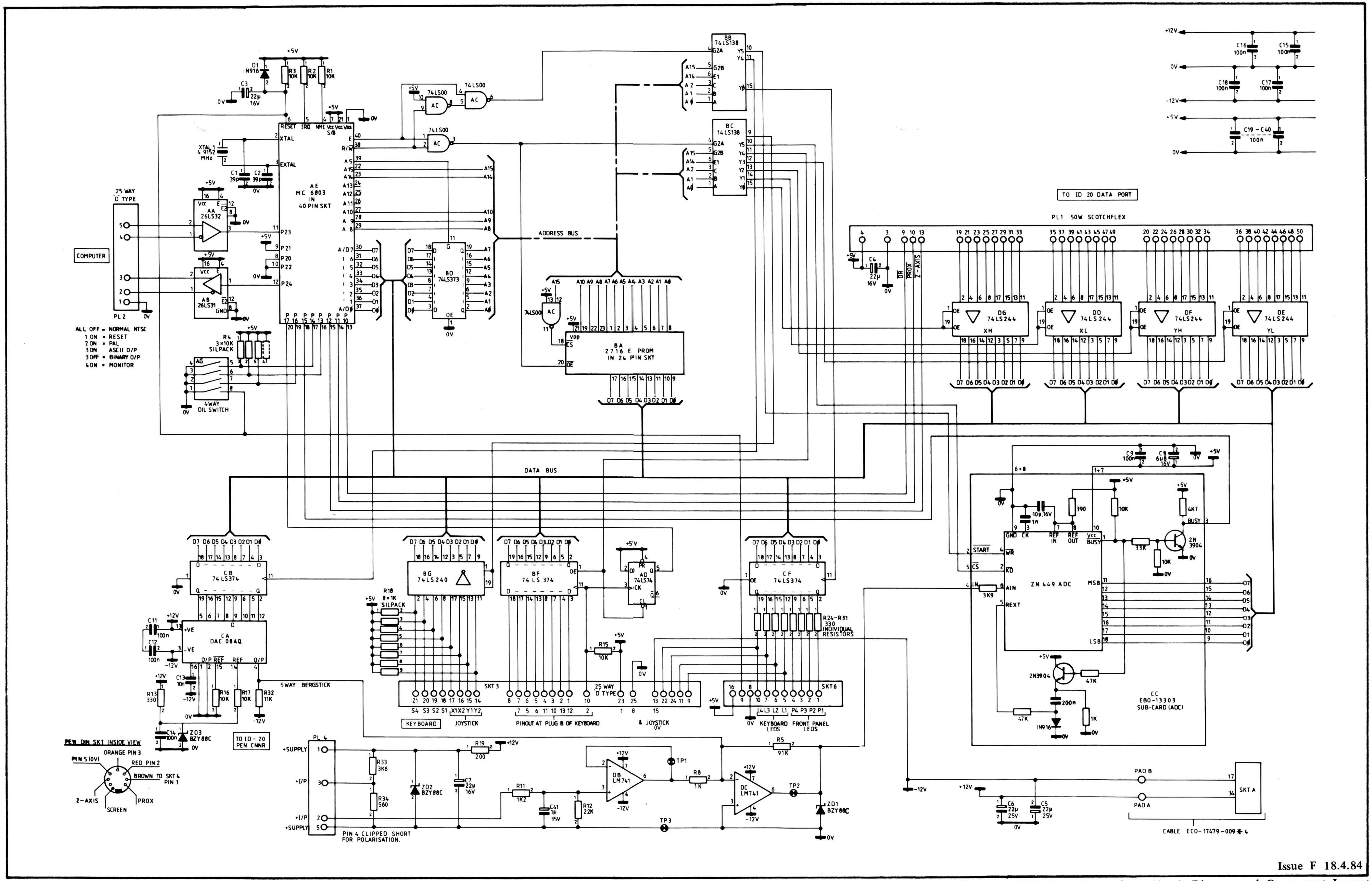
17479, Figure 3 ID20 Control Interface Pen Circuit



17479, Figure 4 ID20 Control Interface Pen Connector Details



17479, Figure 5 ID20 Control Interface Block Diagram



Issue F 18.4.84

17479, Figure 6 ID20 Control Interface : Circuit Diagram and Component Layout

FLOPPY DISC UNIT AND INTERFACE

17446

1. INTRODUCTION

The Quantel floppy disc drive consists of a Shugart 8" double sided double density disc drive, an interface card and a power supply unit. The data format used gives a capacity of about 1.5M bytes with a data rate of 60k bytes/sec. The Interface card makes the drive appear to the system as an SMD device. It may be given any address, although it must physically be the last device because it terminates the 60-way daisy chain cable. The Paintbox software identifies the drive as a floppy only from the configuration switches in the machine. A flag is set which selects the appropriate microcode on the disc sequencer. This is necessary because on a given track the floppy reads first one side of the disc and then the other side (by driving the side select signal) to form a continuous double length track.

2. CIRCUIT DESCRIPTION

The Interface card uses a 6803 microprocessor running software in PROM GD to control the disc drive. It handles the seek operations, monitors the SMD Interface for commands and drives the status signals back to the SMD Interface. When the unit is powered up the processor first executes a 'restore' - a seek to track zero. The processor sets direction (HC pin 6) and sends step pulses via HE pin 8 so that the head is stepped towards the outer edge of disc until the Track Zero signal is received HB pin 5. If this is successful the green LED is lit indicating that the Interface is ready and is waiting for an SMD control signal. The unit only responds to commands if the address corresponds to the unit select data at CB4, CB9, EB9 when Select Tag ED4 is active. The address switches are compared with select data by FA and if correct cause FB to be set by Select Tag, lighting the red 'unit selected' LED. Unit select enables control signal receiver DB and also causes the Interface to drive the SMD status lines on the 60-way cable via BA, CA, DA, EA. The 'Ready' signal from the disc drive (S0) is then passed through to EA pin 12. The drive is only 'Ready' when a disc is inserted and the door is shut. The write protect signal is transferred directly to BA9. To write protect a floppy disc a notch must be uncovered in its cardboard cover. INDEX (TP4, CA12) occurs once a revolution of the disc as a result of the index hole passing a LED and detector in the drive and is used by the Disc Sequencer as the starting point for reading and writing a track.

SMD control signal Cylinder Tag TP5 and Command Tag TP7, are latched in EG and EF. The processor continuously monitors these latches via tristate driver EE to see if a command is received. Cylinder Tag also causes SMD data to be latched in FC. When the processor receives a Cylinder Tag it will de-assert 'ready' and 'on cylinder' and step the drive to the track number in FC. The restore command is directly decoded by GA from D6 via GB pin 2. The write command is also decoded by GA using D0 from GB pin 12 and drives write gate (HE13) directly. HE pin 11 is active low and inhibits stepping of the head. Monostable CG ensures that 'on cylinder' is removed immediately a command is received.

An 8MHz oscillator and counter DE provide a 500kHz servo clock at AG pin 12 which determines the write data rate from the Disc Data Buffer. Data from BE pin 4 is encoded by logic array DF into MFM format. Write precompensation is applied on the inner tracks and is controlled by the COMP input from the processor.

Raw data from the drive is separated into data and clocks by BF, a digital phased locked loop. BG is used to set the data polarity at the start of each track. In MFM coding strings of 1's are indistinguishable from 0's so a period of zero data is recorded at the start of each track as a reference. BG is only enabled when pin 5 of monostable HF is high, a period of ?µs after the index pulse. CG stretches the separated data pulses from pin 7 of BF so that data is clocked into CF producing a serial stream at TP3. Data at AF pin 9 is gated off during the index pulse to avoid spurious data.

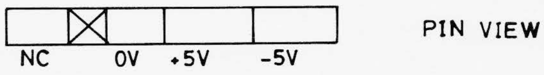
The processor is provided with a serial port which is accessible via the 10-way socket on the Interface card. This is for service use and normally only outputs a start up message. This may be used to verify that the processor is running. Switch 4 of the DIL switch resets the processor when on and allows it to run when off. Switch 5 is normally on but off will select a monitor program on power up.

The Interface card connects to the floppy drive by a 50-way cable. With Issue A Interface cards this cable should have a twist in it. With Issue B cards the cable lies flat.

3. POWER SUPPLY

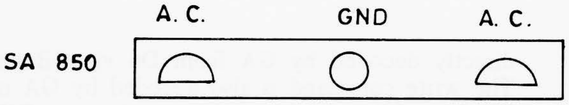
Power is supplied by a switched mode unit SMM50 manufactured by Weir Electronics. The Interface needs +5V and –5V which are provided via the 5-pin connector. Red is +5V, yellow –5V, black 0V.

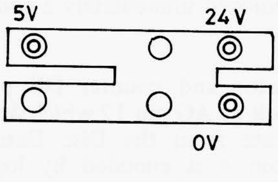
Pin View



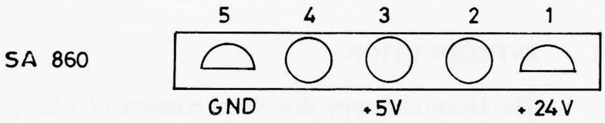
The standard SA850 drive requires +5V and +24V and has a mains motor which is driven continuously. Slimline SA860 drives have a d.c. motor. Blue is +24V. Red is +5V.

Connector Pin View





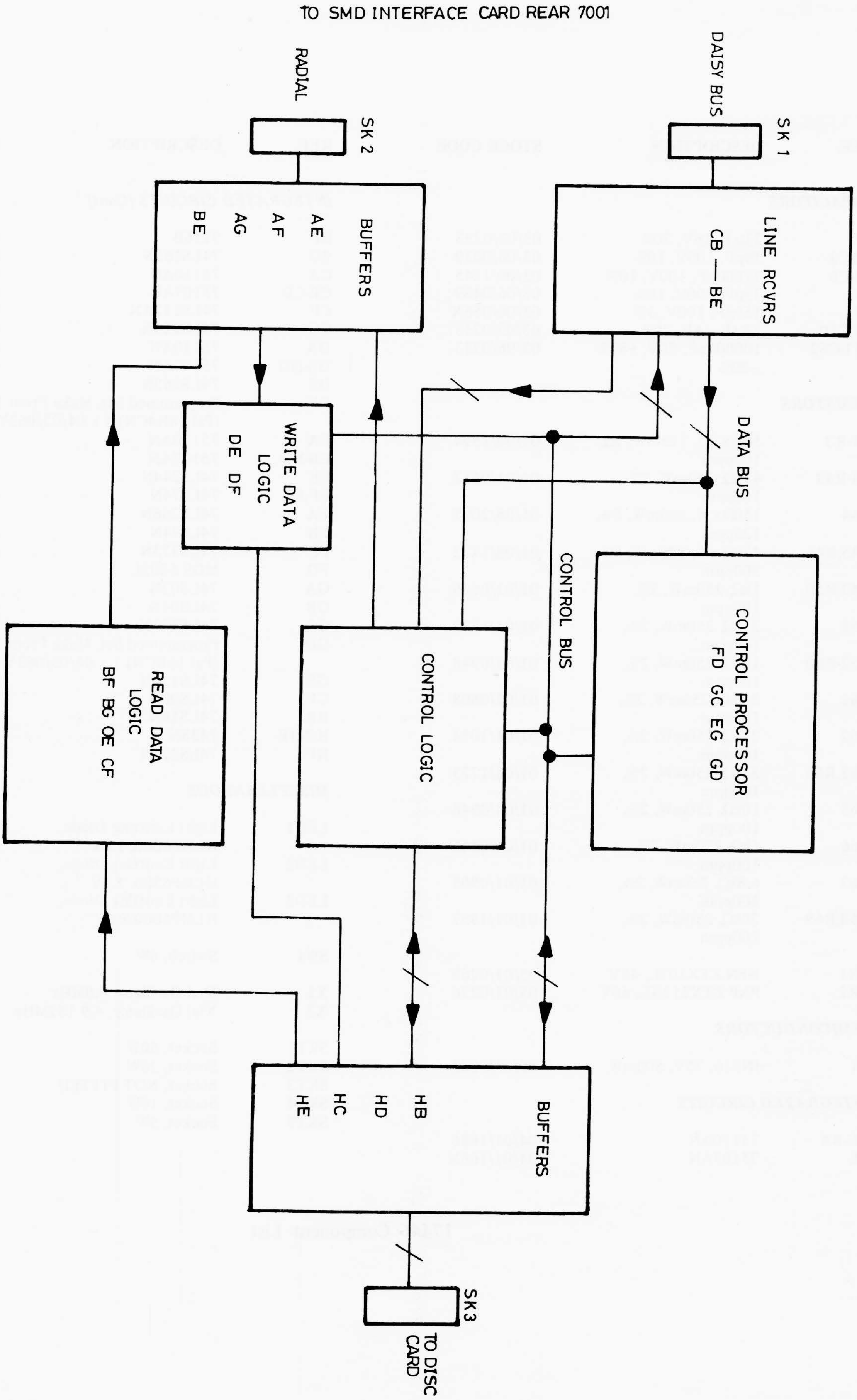
Pin View



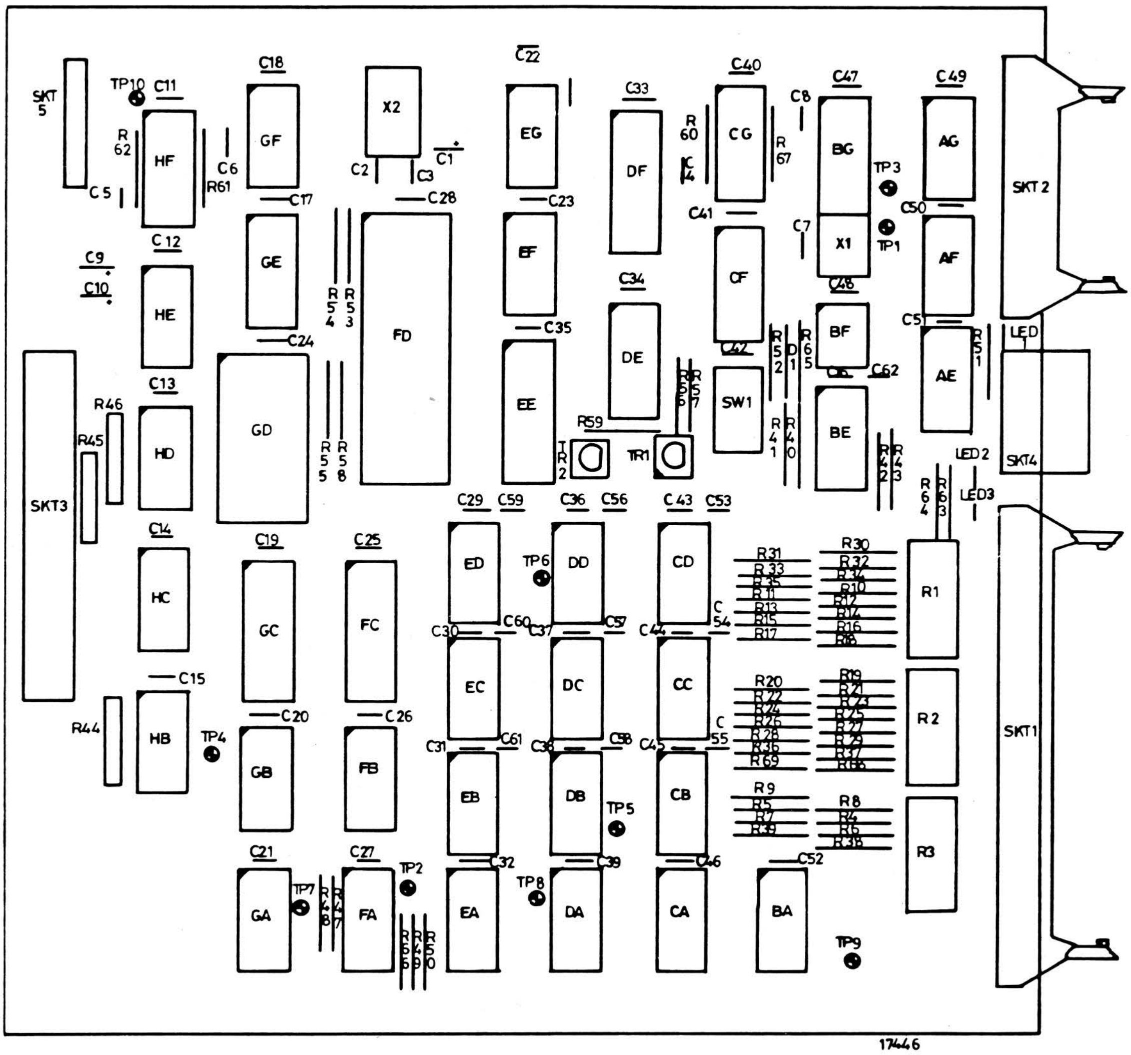
REF.	DESCRIPTION	STOCK CODE
CAPACITORS		
C1	22µF, 16V, 20%	03/03/0253
C2,C3	39pF, 100V, 10%	03/06/0039
C4-C6	27000pF, 100V, 10%	03/00/1245
C7	33pF, 100V, 10%	03/06/0489
C8	150pF, 100V, 5%	03/06/056X
C9,C10	22µF, 16V, 20%	03/03/0253
C11-C62	100000pF, 50V, +80% −20%	03/96/0233
RESISTORS		
R1-R3	56Ω x 15, 125mW, 2Ω, 100ppm	01/08/1594
R4-R43	470Ω, 250mW, 2%, 100ppm	01/01/0557
R44	150Ω x 6, 125mW, 5%, 125ppm	01/08/200Y
R45,R46	470Ω x 6, 125mW, 5%, 300ppm	01/08/1772
R47-R50	1kΩ, 250mW, 2%, 100ppm	01/01/0646
R51	330Ω, 250mW, 2%, 100ppm	01/01/1723
R52-R60	10kΩ, 250mW, 2%, 100ppm	01/01/0948
R61	3.9kΩ, 250mW, 2%, 100ppm	01/01/0808
R62	22kΩ, 250mW, 2%, 100ppm	01/01/1014
R63,R64	330Ω, 250mW, 2%, 100ppm	01/01/1723
R65	10kΩ, 250mW, 2%, 100ppm	01/01/0948
R66	1kΩ, 250mW, 2%, 100ppm	01/01/0646
R67	6.8kΩ, 250mW, 2%, 100ppm	01/01/0905
R68,R69	20kΩ, 250mW, 2%, 100ppm	01/01/1952
TR1	NPN ZTX107L, 45V	05/01/0268
TR2	PNP ZTX212AL, 60V	05/01/0276
SEMICONDUCTORS		
D1	IN916, 75V, 500mW	06/01/0083
INTEGRATED CIRCUITS		
AE-BA	75110AN	04/01/1686
BE	75107AN	04/01/166X

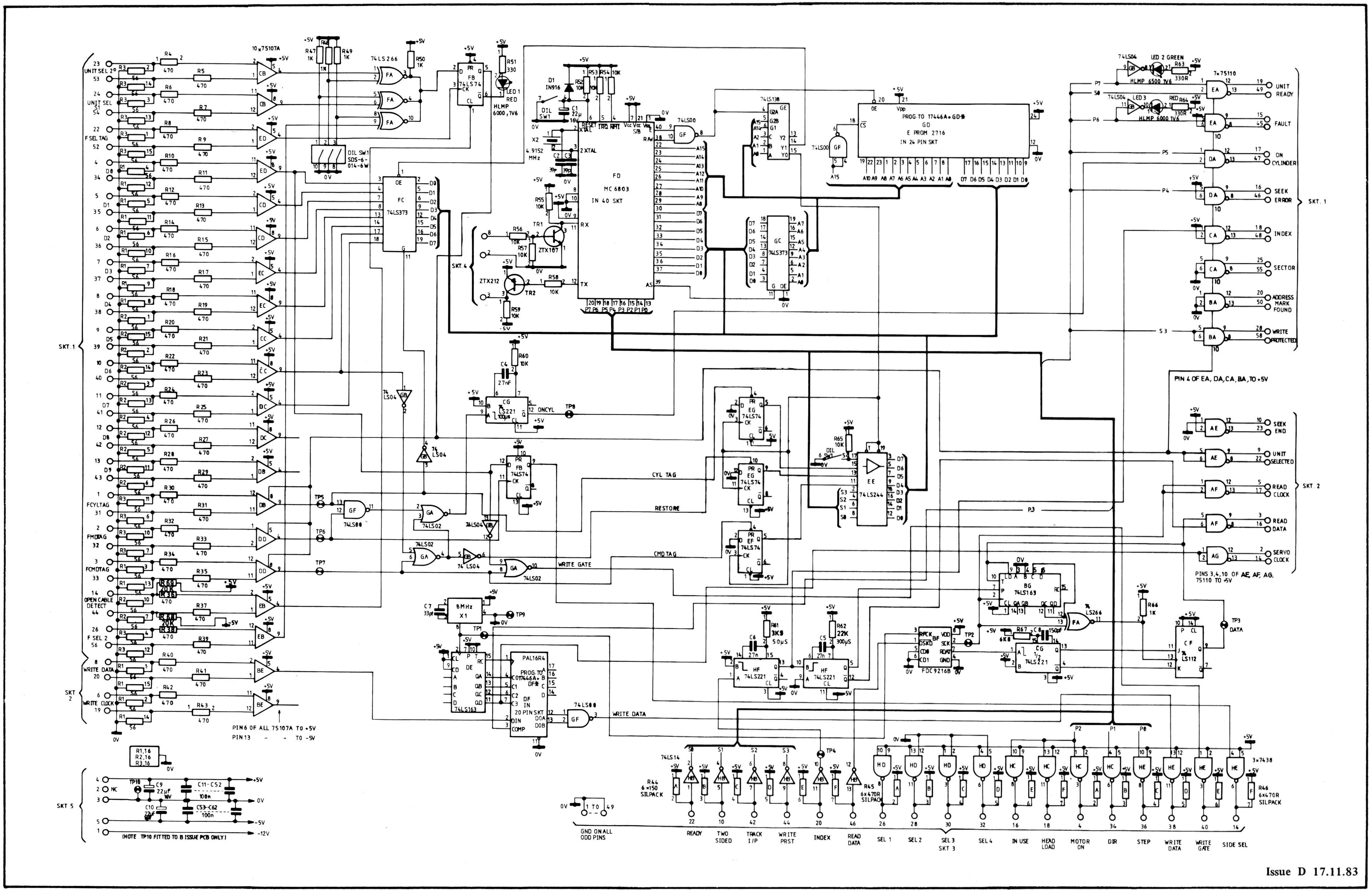
REF.	DESCRIPTION	STOCK CODE
INTEGRATED CIRCUITS (Cont)		
BF	9216B	04/01/7293
BG	74LS163N	04/01/1317
CA	75110AN	04/01/1686
CB-CD	75107AN	04/01/166X
CF	74LS112AN	04/01/6807
CG	74LS221N	04/01/1589
DA	75110AN	04/01/1686
DB-DD	75107AN	04/01/166X
DE	74LS163N	04/01/1317
DF	Programmed Set, Make From 1 x 04/01/5401 (Pal 16R4CN) 1 x 04/03/063Y (MOS 2716J-8)	
EA	75110AN	04/01/1686
EB-ED	75107AN	04/01/166X
EE	74LS244N	04/01/2828
EF,EG	74LS74N	04/01/0728
FA	74LS266N	04/01/2992
FB	74LS74N	04/01/0728
FC	74LS373N	04/01/3921
FD	MOS 6803L	04/03/3469
GA	74LS02N	04/01/1724
GB	74LS04N	04/01/0191
GC	74LS373N	04/01/3921
GD	Programmed Set, Make From 1 x 04/01/5401 (Pal 16RCN) 1 x 04/03/063Y (MOS 2716J-8)	
GE	74LS138N	04/01/109Y
GF	74LS00N	04/01/006X
HB	74LS14N	04/01/3425
HC-HE	7438N	04/01/0507
HF	74LS221N	04/01/1589
MISCELLANEOUS		
LED1	Light Emitting Diode, HLMP6000, 1.6V	06/03/030Y
LED2	Light Emitting Diode, HLMP6500, 1.6V	06/03/0327
LED3	Light Emitting Diode, HLMP6000 1.6V	06/03/030Y
SW1	Switch, 6W	26/06/0184
X1	Xtal Oscillator 8.0MHz	28/02/0295
X2	Xtal Oscillator, 4.9 152MHz	28/01/0397
SKT1	Socket, 60W	08/18/0784
SKT2	Socket, 26W	08/18/0938
SKT3	Socket, NOT FITTED	
SKT4	Socket, 10W	08/18/0091
SKT5	Socket, 5W	08/07/149Y

17446 Component List



17446, Figure 1 Floppy Disc Interface Card Block Diagram


SKT 5
TP10
C11
C18
X2
C22
C33
C40
C8
C47
C49
R 62
HF
GF
C6
R61
C2
C3
C1
EG
DF
R 60
CG
R 67
BG
TP3
AG
SKT 2
C5
C17
C28
C23
C 14
C41
C7
X1
TP1
C50
C12
GE
R 54
R 53
FD
EF
C34
CF
AF
C9
C10
HE
C24
C35
C48
BF
C51
LED 1
C13
GD
EE
DE
C42
R 52
D 1
R 65
C62
AE
R46
R45
R 55
R 58
R59
R 56
R 57
SW1
R 41
R 40
BE
R 42
R 43
R 51
SKT4
LED 2
HD
TR 2
TR1
C16
R 64
R 63
LED3
SKT3
C29
C59
C36
C56
C43
C53
C14
C19
C25
ED
TP6
DD
CD
R31
R33
R35
R11
R13
R15
R17
R30
R32
R34
R10
R12
R14
R16
R18
R1
HC
GC
FC
C60
C37
C57
C 54
C30
C44
C15
EC
DC
CC
R20
R22
R24
R26
R28
R36
R69
R19
R21
R23
R25
R27
R29
R37
R66
R2
SKT1
C20
C26
R44
HB
TP4
GB
FB
C31
C61
C38
C58
C45
C 55
EB
DB
CB
TP5
R9
R5
R7
R39
R8
R4
R6
R38
R3
C21
C27
TP2
C32
C39
C46
C52
TP7
R 48
R 47
GA
FA
TP8
EA
DA
CA
BA
TP9
R 65
R 46
R 59
R 50
17446



Issue D 17.11.83

17446, Figure 2 Floppy Disc Interface Card : Circuit Diagram and Component Layout

POWER SUPPLY

1. GENERAL

The power supply is a modular switched mode unit manufactured by Gould Electronics and known as a HIFLEX supply. The supply plugs into the back of the mainframe and is held in position by four screws. Extender cables are provided which allow the unit to be operated outside the crate with access to the backplane wiring. Care must be taken when doing this since the mains supply is then along one of the extender cables. The supply provides +5V, –5V and ±15V. The 15V supplies are used to drive regulators mounted on an external heatsink to provide ±12V. On each circuit board the power supplies are on the following edge connector pins.

AB1,2	0V
AB4	+12V
AB5,6	+5V
AB7	–5V
AB8	–12V
AB59,60	0V
AB10	analogue 0V

The d.c. supply voltages on full load should be checked occasionally on the following cards. Measure with an extender card in the slot but without the card fitted.

I/P Timing	+5V	set to 4.98 ±0.02V
O/P Locking	+5V	should be <4.92
	–5V	set to –5 ±0.03V
	+12V	set to 12 ±0.02V
	–12V	set to 12 ±0.02V

I/P Locking as for O/P Locking

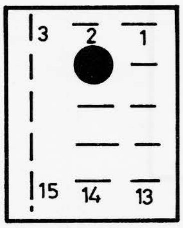
The +5V and –5V supplies require adjustment of the preset potentiometers on the HIFLEX unit. These are only accessible with the supply on the extenders. The ±12V supplies are adjusted by potentiometers on the bottom of the external heatsink. See Figure 1.

The total current drawn at 5V is about 45A - well within the capability of the supply (90A).

At 240V about 2 - 5A is drawn by the machine at full load. The mains fuse is 20mm 5A for 240V and 1" 10A for 110V machines. The power supply has its own 20A HRC fuse.

2. CONNECTIONS TO POWER SUPPLY

Connector Pin View



There are two connectors the top one is referred to as SKT35 and the bottom as SKT36.

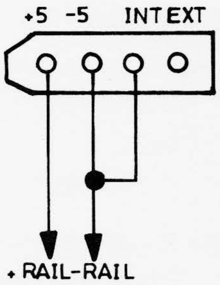
Switched mains line	SKT35-1	to	Terminal Block-1
Switched mains neutral	SKT35-3		Terminal Block -5
Earth	SKT35-5		Earth Terminal
+5V Red	SKT35-4		E2-A5
+5V Red	SKT35-7		E8-A5
+5V Red	SKT35-10		E15-A5
+5V Red	SKT35-13		E21-A5
+5V Red	SKT35-2		E27-A5
0V Black	SKT35-6		E2-A1
0V Black	SKT35-9		E8-A1
0V Black	SKT35-12		E15-A1
0V Black	SKT35-15		E21-A1
0V Black	SKT35-8		E27-A1
+5V Sense +ve	SKT35-14		E18-A5
+5V Sense –ve	SKT35-11		E18-A1
–5V Yellow	SKT36-13		E3-A7, E26-A7
0V Black	SKT36-10		E3-A1, E26-A1
–5V Sense –ve	SKT36-7		E14-A7
–5V Sense +ve	SKT36-4		E14-A1
+12V Or/Red	SKT36-14		E16-A4, E35-A4
0V Black	SKT36-11		E16-A1, E35-A1
+12V Sense +ve	SKT36-8		E12-A4
+12V Sense –ve	SKT36-2		E12-A1
–12V Grey/Blue	SKT36-12		E17-A8, E36-A8
0V Black	SKT36-15		E17-A1, E36-A1
–12V Sense –ve	SKT36-6		E12-B8
–12V Sense +ve	SKT36-9		E12-B1

3. HIFLEX UNIT DESCRIPTION

The Hiflex system consists of an input module which produces a switching waveform of 350V p-p at about 30kHz and a number of output modules. The unit used in the DPB 7000/1 consists of:

Module Type	HO5-30	5V 30A	(–5V)
	HO15-10	15V 10A	(+15V)
	HO15-10	15V 10A	(–15V)
	HO5-90	5V 90A	(+5V)

All output modules are fully protected for overvoltage and current limit. A green LED on each module indicates correct output. The 5V 90A module has temperature sensors which trip all outputs in the event of excessive temperature. The unit is rated at 70°C. Remote sensing is provided to compensate for voltage drop in the power leads. The same connections to each module are:



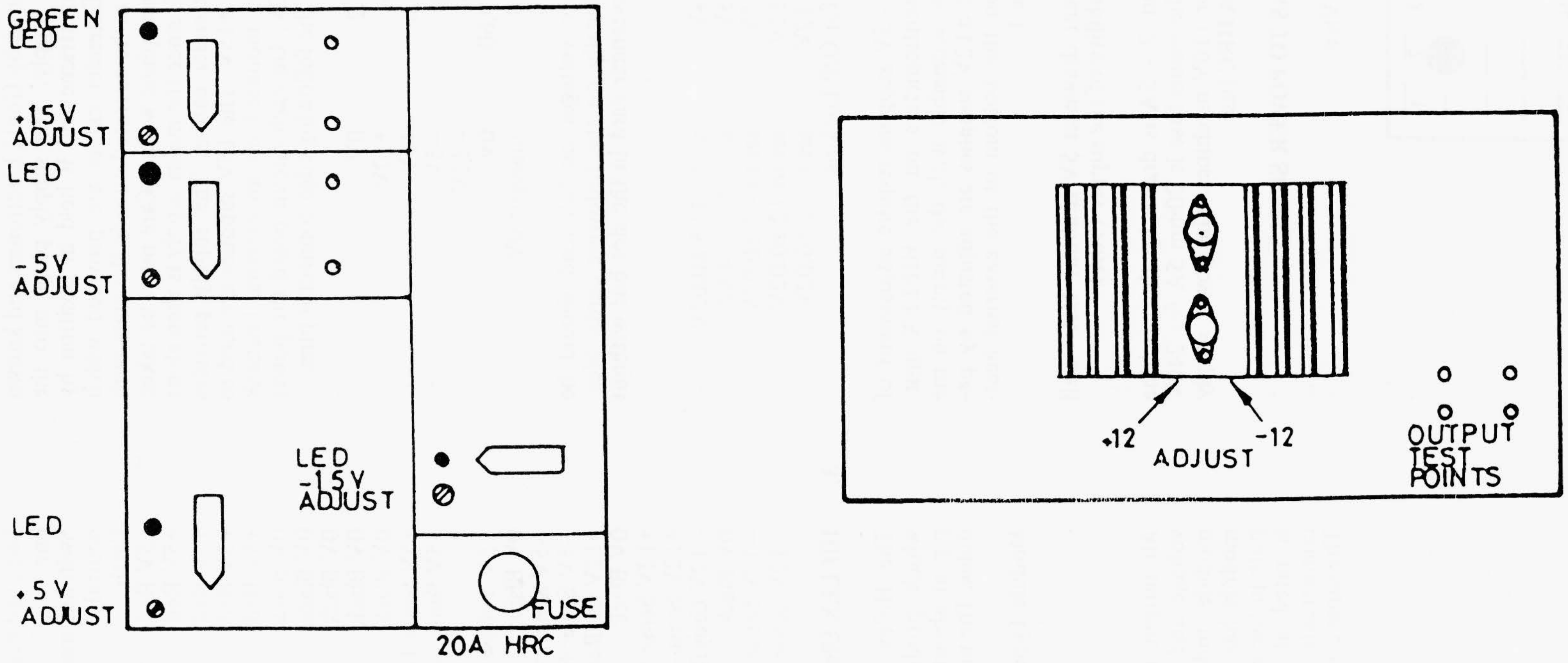


Figure 1 Location of Power Supply Adjustment Potentiometers

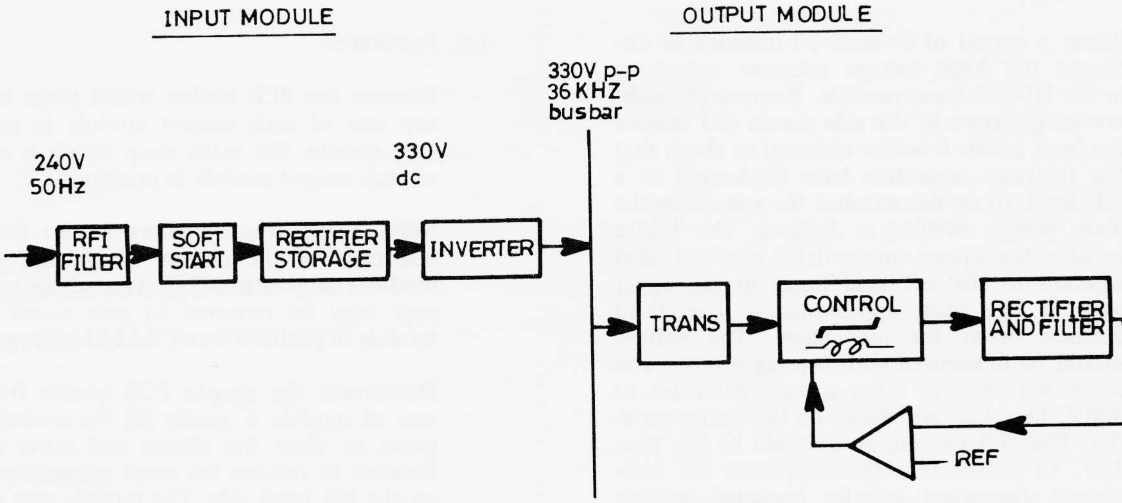


Figure 2 Power Supply Block Diagram

The block diagram Figure 2 shows the basic components of a Hiflex system, comprising the 750W input module feeding the central busbar and one output module. The main busbar between input and output can be at a frequency of around 25kHz and a peak to peak voltage of 260V (180V a.c. input) up to a frequency of 36kHz and a peak to peak voltage of 370V (264V a.c. input). The individual output modules are all fitted with high frequency transformers for isolation and to prevent interaction between output modules. The main control is provided by a magnetic amplifier with simple linear control circuitry to provide the necessary regulation.

4. HIFLEX SYSTEM FAILS TO POWER UP CORRECTLY

(a) Check that the input fuse is the correct value (20A) and has not blown. Also ensure that the unit is set at the correct voltage setting for the appropriate a.c. line input voltage being applied. If the a.c. line voltage is below 65% of its nominal value, the undervoltage circuit in the HI 750 stage of the system will be activated and will prevent operation of the system.

(b) Disconnect all external load leads from each output module. If remote sensing is being used, make the local sense connections with the 4-way Molex connector on each output module.

(c) Allow the unit to cool down for a period of 30 minutes, and check for any obstructions around the air intake and exhaust slots. The unit is fitted with overtemperature sensors on the HI 750 input module, 300W and 450W output modules. Any overtemperature condition in any of these three areas will cause the complete system to shut down.

(d) Apply the appropriate a.c. line voltage and check that the fan is working. This will confirm that the input fuse, filter and soft start circuit are working correctly. Check the 'OUTPUT UP' LED on each output module, if any one of these is not illuminated, it signifies that a fault condition exists on that particular output module. With a multimeter set to the appropriate d.c. voltage range, monitor the voltage present on the output terminal busbar of each module. These should be stated on the label on the Hiflex top cover. Ensure making this check that all 4-way Molex connectors are fitted, and all screws on busbars are tight.

(e) If none of the 'OUTPUT UP' LEDs is illuminated and the fan is working, it signifies either that a fault exists on the HI 750 module, or that a fault condition on one output module has caused the inverter to shut down. In this case, the a.c. input supply should be removed for at least three seconds in order to reset any fault condition. It is now necessary to isolate the area where the fault condition exists. This can be achieved by observing the 'OUTPUT UP' LEDs at the moment of switch on. Apply the a.c. input supply and observe the 'OUTPUT UP' LEDs. If they are illuminated for a brief period and are then extinguished, a fault condition is indicated on one of the output modules. To isolate the faulty output module it is necessary to remove each in turn and to repeat the 'switch-on test' observing that 'OUTPUT UP' LEDs. The faulty module should then be replaced.

If none of the 'OUTPUT UP' LEDs is briefly illuminated at switch on, the fault condition is associated with the HI 750 input module and this should be replaced.

5. MODULE REPLACEMENT

(a) Output Modules

To replace a faulty output module the following procedure should be followed with all external connections removed:

Allow a period of at least 30 minutes to discharge the high voltage reservoir capacitors in the HI 750 input module. Remove the eight retaining screws in the side panels and remove the back cover. It is now essential to check that the reservoir capacitors have discharged to a safe level, to do this monitor the voltage on the main bridge rectifier as follows. The bridge rectifier is a square encapsulated block situated adjacent to the left-hand panel in the upper part of the unit, approximately one third distance from the rear panel. The voltage should be monitored with top tag positive and lower tag negative using a multimeter set to 300V, four tags are visible on the bridge rectifier. The voltage measured should be less than 30V; to ensure that the capacitors are completely discharged a fully insulated resistor of value 1000 ohms should be applied across the bridge rectifier positive and negative.

(b) Positions 1-5

Remove the PCB Busbar which plugs into the top rear of each output module in positions 1-5. Remove the earth strap which is screwed to each output module in positions 1-5.

The module may now be removed by gently lifting the front panel and removing forwards when clear of the chassis lip.

(c) Position 6

Remove the PCB busbar which plugs into the top rear of each output module in positions 1-5, remove the earth strap which is screwed to each output module in positions 1-5.

Remove the four retaining screws from the underside of the chassis which supports the modules in positions 1-5. This whole assembly may now be removed to gain access to the module in position 6 and HA1/HA2 boards.

Disconnect the plug-in PCB busbar from the rear of module 6, gently lift the module front panel to clear the chassis and move slightly forward to remove the earth connection screw on the left hand side. The module may now be removed.

(d) Re-Assembly

Follow the reverse of the above procedure to re-assemble the Hiflex system noting that each output module has location spigots which fit into slots on the mainframe, ensure that all plugs are refitted in the correct positions and are pushed fully home.

The electrical performance of the unit should now be checked in accordance with the test procedure.

DIGITAL INTERFACE CARD

17480

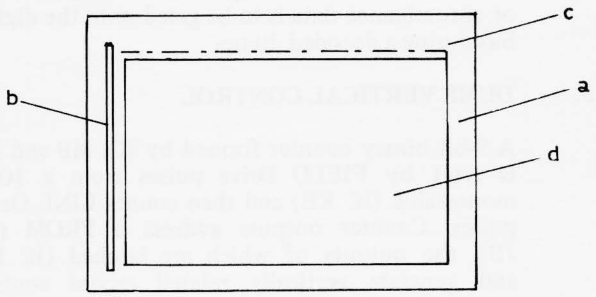
1. GENERAL

The Digital Interface can be divided into three circuit elements.

(a)	Dump	Output video generation from picture data.
(b)	Load	Recovers picture data from input video.
(c)	Computer Interface	Receives and decodes processor commands.

2. DATA FORMAT

Data from the buffer is encoded into standard video format, each field taking forms shown below:



(a) Black Background

(b) LINE SYNC BAR

Lines 23 to 248 (285 to 510)
[Lines 29 to 294 (341 to 606)]

(c) FIELD SYNC LINE

Line 25 (287)
[Line 31 (343)]

(d) DATA

Lines 31 to 246 (293 to 508)
[Lines 37 to 292 (349 to 604)]

The white LINE SYNC BAR (b) is used to synchronise replay data recovery circuits. A FIELD SYNC LINE (c) is present only on fields with data and synchronises replay vertical circuits.

DATA AREA (d) consists of NTSC 216 lines [PAL 256 lines] with NTSC 13 bytes [PAL 18 bytes] of eight data bits with parity on each line. Data is output in serial form, MSB first, binary 1 being video white and a 0 black. Eight bits of data are followed by a modified even parity bit, the 'all ones' case generating odd parity to ensure detection of tape dropouts to either limit. Each bit cell is NTSC 420ns wide derived from 6 x 4fcs periods [PAL 296ns wide derived from 4 x video sample periods]. This modest data rate (maximum 1.7MHz) of below sub-carrier frequency ensures the video output is recorded predominantly as luminance on a VTR, avoiding modifying chrominance paths.

To further reduce the signal bandwidth video black to white and white to black transitions have an intermediate grey value which increases rise and fall times.

Each data field output NTSC 2808 bytes (216 lines of 13 bytes), so 133 video fields are used to output one picture of 317,712 bytes (768 pixels x 484 lines) in encoded form. In PAL each data field outputs 4608 bytes (256 lines of 18 bytes), so to output a picture of 897,024 bytes (768 pixel x 584 lines x 2 since luminance and chrominance are separate) 195 video fields are used.

Data fields for a particular picture are output consecutively and are proceded by a PICTURE SYNC FIELD, which consists of a data field with FIELD SYNC LINES in the data area. Interpicture periods output fields without a FIELD SYNC LINE and an IDLE pattern in the data area.

Each picture is preceded with a TITLE BLOCK consisting of a PICTURE SYNC FIELD and a single DATA field.

When loading pictures, recovered data is checked for errors, and incorrect bytes replaced by a concealment circuit. To aid error detection each byte has a parity bit. A noise circuit in Input Locking card EBO 17564 checks for abnormal black and white periods and in NTSC alternate bytes are inverted to detect major horizontal shifts. Bytes preceding and suceeding a byte in error are also replaced.

3. DUMP CIRCUITS

Line and Field drives and H-locked video sample rate clocks from the Output Timing card EBO 17418 are used to generate horizontal and vertically related waveforms.

4. DUMP HORIZONTAL CONTROL

A 10-bit binary counter formed by IC's DE, CE and EE, is reset by Line Drive pulses from a $3\mu s$ monostable IC KE and then counts H-locked sample pulses NTSC 14.318MHz [PAL 13.50-MHz]. The nine most significant bits of this counter address a patter generating PROM (IC AE) the outputs of which are latched (IC BE). Eight horizontally related waveforms are produced:

(a) Record Control A

(b) Record Control B

(c) Serialiser Shift Clock

(d) Serialiser Load Clock

(e) IDLE Pattern

(f) Multiplex Control

(g) Clock A

(h) Clock B

Record control signals A and B are combined with vertical and field signals in PAL (IC DC) to format the video data output. They control the Black - Sync BA - Black - Data True/Invert structure each line. Refer to horizontal waveform diagrams.

Record control A also controls NTSC byte insertion such that alternate bytes are inverted, and also provides the Field Sync Line pattern of alternate bytes of NTSC 11111111.0 and 00000000.1. [PAL 11110000.0 and 00001111.0.]

The IDLE pattern replaces picture data during inter-picture fields. It consists of NTSC 13 bytes [PAL 18 bytes] of 10101010 (parity 0); the 'average video' nature of this signal ensures recorder or monitor sync separator circuits with adaptive slicing remain benign.

An eight-bit parallel load shift register (IC CD) is loaded by Serialiser LOAD Clock with data from the digital bus. Nine bits are shifted out of the register by Serialiser SHIFT Clock at one bit-cell intervals NTSC 420ns [PAL 296ns]. An even parity generator (IC DD) output is presented to the serial input of the serialiser and becomes the ninth bit. Parity is modified by the 'all ones' case, detected by an eight-input NAND gate IC EB.

Clock A and Clock B are data request clocks for frame store picture data to be made available on the digital bus, either directly from two buffers (IC's AD and BB) in luminance and chrominance for a decoded dump, or from the Encoder EBO 17481 for an encoded dump.

Two clocks A and B are required because the number of luminance/chrominance byte pairs required for a decoded dump in NTSC format varies from seven on one line to six on the next, because there are 13 bytes per line.

A multiplex control signal is generated to control, with an odd/even line signal, whether luminance or chrominance data is to be gated onto the digital bus during a decoded dump.

5. DUMP VERTICAL CONTROL

A 9-bit binary counter formed by ICs MB and LB is reset by FIELD Drive pulses from a 10µs monostable (IC KE) and then counts LINE Drive pulses. Counter outputs address a PROM (IC JB), the outputs of which are latched (IC IB) and generate vertically related record control signals C and D. The following vertical structure is produced:

	NTSC Line No.	PAL Line No.	C	D
BLACK	1 – 22	1 – 28	0	0
LINE SYNC BAR only	23 – 24	29 – 30	1	0
LINE SYNC BAR with FIELD SYNC LINE	25	31	1	1
LINE SYNC BAR only	26 – 30	32 – 36	1	0
LINE SYNC BAR with DATA	31 – 246	37 – 292	0	1
LINE SYNC BAR only	247 – 248	293 – 295	1	0
BLACK	249 – 262	296 – 312	0	0

Table 1 Vertically Related Record Control Signals

6. DUMP FIELD CONTROL

Two D-type bistables (IC EC) form a 2-bit limiting counter. This counter is RESET and ENABLED under processor control and is clocked by FIELD drive pulses. Its two outputs, RECORD control E and F, generate field related sequence:

	E	F
Inter-picture (IDLE) Fields	0	0
Picture-Sync Field	1	0
Data Fields	1	1

7. DUMP VIDEO GENERATION

Serialised data, IDLE pattern and internally generated '0' and '1' are gated with horizontal AB, vertical CD and field EF control signals in a PAL (IC DC). These signals generate the video format for picture dumping. One of four tristate outputs is enabled depending on NTSC/PAL and DATA/TEST control signals. This output is latched and buffered to drive a video output stage on Output EBO 17449.

An ACTIVE LINE signal is also generated and used to gate data requests from the framestore.

8. DUMP CLOCK CONTROL

A PAL (IC CC) generates a Dump data request clock DCLK, to read data from the framestore onto the Brush Bus. This request clock is derived from horizontally generated pulses Clock A and Clock B, together with NTSC/PAL, mode and multiplexer gating signals as shown in the Table below.

If decoded data is being dumped PAL (IC CC) generates two enable signals. ENLUM and ENCHR to gate either luminance or chrominance data from the framestore (via Brush Bus) onto the Digital Bus and serialiser. Luminance is gated by IC AD and chrominance IC BB.

When dumping encoded data the Encoder EAO 17481 output is enabled via buffer AC and decoded data paths disabled.

9. LOAD CIRCUITS

During a LOAD operation previously dumped pictures are recovered and written into a framestore and then transferred to disk.

Input Locking card EAO 17564 provides sliced, time-corrected data a noise signal and time and field synchronisation signals.

Serial data is clocked into a shift register (IC GD) at video sampling rate NTSC 14.318MHz [PAL 13.50MHz]. Parallel outputs of the register feed a PAL (IC FD) which performs several functions:

(a) Positive Edge Detector - black to white transitions.

(b) Negative Edge Detector - white to black transitions.

(c) Data - corrected for polarity and phase.

Positive edge data transitions are gated with a line drive derived window for horizontal synchronisation. Negative data edges are used in a data quality circuit to optimise video level controls. Serial data is phase shifted by selection of shift register output and polarity corrected by inverting alternate bytes, as controlled by polarity input. Within the PAL an R-S bistable is formed by cross-coupling gates, which is reset at the start of each byte and set by the Noise input.

10. LOAD HORIZONTAL CONTROL

A 10-bit binary counter (ICs JC, IC and KC) with a count limit of NTSC 910 [PAL 864] clocks is clocked by video sample rate pulses NTSC 14.318-MHz [PAL 13.5MHz]. Two signals can load this counter with its reset value:

(a) Counter ripple carry, or,

(b) synchronisation pulse.

DECODED NTSC	LUM + CHR	Odd Lines Even Lines	Clock A Clock B
DECODED PAL	LUM + CHR	All Lines	Clock A
or DECODED NTSC PAL	LUM ONLY	All Lines	Clock A or Clock B
or ENCODED NTSC PAL	LUM + CHR	All Lines	Clock A or Clock B
or ENCODED NTSC PAL	LUM ONLY	All Lines	Clock A or Clock B

Multiplexing Gating Signals

A horizontal synchronisation pulse is generated by gating positive edge pulses with a window signal which is derived from a 1.5µs monostable (IC MA) triggered from an adjustable line-drive delay (monostable IC MA, 9 to 13µs set by VR1).

The function of this circuit is to detect the black to white transition of the Line Sync Bar within a window and then 'crash lock' the horizontal counter. This provides phasing of the counter with incoming serial data.

Counter outputs (nine MSBs) address a PROM (IC HC), the outputs of which are latched (IC GC) and provide eight horizontally related signals locked to incoming data.

(a) Clock A
Byte store clocks
(b) Clock B

(c) Clock L - Latch Clock

(d) Clock Q - Quality Detect Clock

(e) Noise Reset - To reset Noise Detect bistable

(f) Polarity - Invert alternate bytes of NTSC encoded data

(g) Byte Clock - Byte register LOAD clock, eight data bits and parity

(h) Bit Clock - Deserialiser SHIFT clock

Deserialiser Bit Clocks are phased to occur at the mid-point of incoming bit cells and clock a shift register (IC FC) for bit serial to byte parallel conversion of data. After eight SHIFT pulses for DATA a LOAD pulse in the parity bit position broad-side loads data from the shift register into a holding latch (IC FB) and loads the parity bit into a bistable (IC JA).

A parity checker (IC GB) generates a correct/error signal from eight data bits and one parity bit. This signal, together with eight data bits and the NOISE DETECT signal feed a PAL (IC HB) which provides a composite error signal and a field sync line detector.

Data is considered good if the following conditions are met:

(a) PARITY correct.

(b) Special case 'all ones' correct.

(c) Within active data area of incoming video.

(d) Noise not detected.

For good data recovery the input video must be sliced at the correct level. The adaptive slices on the Input Locking card EBO 17564 should maintain this condition. This can be checked by effectively checking the duration of the whole LINE SYNC BAR.

When set correctly the LINE SYNC BAR has a white period of NTSC 840ns [PAL 890ns] six horizontal PROM periods. This fact is used to give a data quality indication (green LED) used by horizontal PROM output Data Quality pulse, which is locked to the LINE SYNC BAR positive edge, clocking a D-type bistable (IC KA) with data from the negative edge detector.

11. LOAD VERTICAL CONTROL

A 9-bit binary counter (ICs JD, ID and KD) is reset by FIELD drive pulses from a 10µs monostable (IC LA). Counter outputs address a PROM (IC HD), the outputs of which are latched (IC GE) and provide four vertically related signals:

	NTSC Vertical Counter		PAL Vertical Counter	
	Sync Det.	No Sync	Sync Det.	No Sync
(a) Active Data Lines	#204 –	2DB –	#204 –	303 –
(b) Non Data Field	–	16	–	16
(c) Data Field	20A	–	20A	–
(d) Sync Window	1 – n	1 – B	1 – n	1 – B

N.B. n is a maximum of #B in fields where a field sync line is detected.

When a data FIELD SYNC line is detected and falls within the SYNC WINDOW signal the vertical counter is loaded with #200 causing the system to hop-lock. If a FIELD SYNC line is not detected the counter continues to NTSC #106 [PAL #138].

An active DATA LINE signal occurs during lines which contain encoded picture data and is used to gate horizontally generated framestore write pulses. Either a DATA FIELD or NON-DATA FIELD pulse occurs 12 lines after the SYNC line, which is convenient time to check the status of incoming fields i.e. whether it is DATA, Picture-Sync or Interpicture Field.

12. DATA SYNC DETECTION

During a LOAD operation several levels of synchronisation have to be achieved for correct picture data recovery:

(a) BIT BYTE - Horizontal crash-lock from SYNC BAR.

(b) DATA AREA - Vertical hop-lock from FIELD SYNC LINE.

(c) PICTURES - Field sequence from PICTURE SYNC FIELD.

Three types of field have to be detected.

(a) DATA Field

With FIELD SYNC LINE and picture information in DATA area.

(b) PICTURE SYNC Field

With FIELD SYNC LINE and FIELD SYNC LINE pattern repeated in DATA area.

(c) INTER-PICTURE Field

No FIELD SYNC LINE and IDLE pattern repeated in DATA area.

Data FIELD SYNC LINES consist of NTSC thirteen byte of alternate bytes of 11111111.0 and 00000000.1 [PAL eighteen bytes of alternating 11110000.0 and 00001111.0]. This sequence is detected by logic within PAL (IC HB), gates form a cross-coupled bistable which is set by detecting one byte pattern and reset by the other, producing a waveform which toggles during a FIELD SYNC LINE. A counter (IC LD) is preset with NTSC 2 [PAL 0] by LINE drive pulses and then counts negative transitions of the bistable output. If the most significant bit of the counter is set i.e. NTSC six to thirteen [PAL eight to fifteen] negative transitions have occured on a line, this is deemed to be a FIELD SYNC LINE. Another counter (IC MC) is reset by FIELD drive pulses and counts FIELD SYNC lines is used to detect a PICTURE SYNC Field. Bit three of this counter i.e. eight to fifteen, is gated with DATA FIELD pulses which sets a PICTURE SYNC bistable (IC JE).

If PICTURE SYNC bistable is set, the next FIELD drive pulse sets a DATA FIELD bistable (IC JE) which is used to gate framestore write pulses.

If is necessary to know when picture DATA fields have ended, i.e. a complete picture has been recovered. DATA fields are followed by IDLE inter-picture fields without a FIELD SYNC LINE. Non DATA FIELD pulses are produced during IDLE fields and are used to reset the PICTURE SYNC and DATA FIELD bistables.

13. LOAD LIMITS

For successful picture loading replay digital video must be synchronised within horizontal and vertical limits.

Data tapes should be replayed with the same picture position as a dump. A special line time base corrector in Input Locking card EBO 17564 retimes data on a line by line basis.

Horizontally, the SYNC BAR positive edge must occur within a 1.5µs window. This can be checked during a LOAD by monitoring POS. EDGE (TP2), the first pulse of each line should be in the centre of the LINE SYNC window (TP1). This condition is best optimised by externally adjusting a picture phase of the video source. Alignment can be achieved by adjusting a LINE drive delay VR1, but this is factory preset for back-to-back mode.

Vertically, the FIELD SYNC LINE must occur within a line window.

An error indicator (LED 6) will glow depending on error rate, it should normally be off when good data is being recovered.

14. LOAD CLOCK CONTRAST

The transfer data into framestore byte clocks generated by the horizontal counter and PROM are gated within a PAL (IC ED) depending on the data mode.

Decoded	NTSC	Lum + Chr	Odd Lines Even Lines	Clock A Clock B
Decoded	PAL	Lum + Chr	All Lines	Clock A
Decoded	NTSC or PAL	Lum Only	All Lines	Clock A or Clock B

Multiplexing Gating Signals

Encoded	NTSC or PAL	Lum + Chr	All Lines	Clock A or Clock B
Encoded	NTSC or PAL	Lum Only	All Lines	Clock A or Clock B

Multiplexing Gating Signals (Cont.)

Clocks are also gated by

(a) Active Data Lines - vertically generated

(b) Data Field - field signal

(c) Absorb

Since data is delayed by one byte for error concealment the store clocks are also delayed. This is done by absorbing the first clock. A shift register (IC LD) is reset at the start of each picture and shifts in a '1' at each clock pulse. The QA output is used to gate store clocks.

15. CONCEALMENT

If a byte from Digital Input is faulty i.e. incorrect parity or noise, it can be replaced with data from the picture line above. A RAM (IC EA) stores either one or two lines of picture information, which is updated with good data and read to replace faulty bytes. A line picture point counter (ICs CA, FA, and HA) address the RAM. In NTSC encoded mode either a count limits of 766 for a Field or 1534 for a Frame picture is used to correct for sub-carrier phase shifts. In PAL decoded mode the line counters is reset each line by a pulse from the Brush Address card.

When a byte is detected as faulty it is replaced together with bytes preceding and succeeding it. To enable preceding bytes to be replaced a one byte delay is introduced into the data path (IC DB).

Concealment is controlled by a PAL (IC FE) and an error shift register (IC HE). Byte error status from PAL (IC HB) is clocked into a 3-bit error shift register the outputs of which feed the concealment control PAL. Concealment can be switched OFF under processor control or an on-board switch (SW1-1), this condition is indicated by LED 7.

16. PROCESSOR CONTROL

The DPB 7000/1 processor controls the Digital Interface, Encoder and Decoder via the main processor highway.

Processor commands are decoded by a PAL (IC AA) which generates data strobes and enables:-

(a) Command Strobes

(b) Status Read

(c) Resets

Processor CSR code 13 has been allocated to the Digital Link system cards. Refer to Table 1 for control word details.

Command Strobe CMD clocks the bottom eight bits of the processor word into a register (IC CA). The clock is decoded from a Write to CSR 13 with data bits 15 hi and 14 lo.

Status Read RDS enables the output of a buffer (IC BA) which drives eight bits of status data onto the processor bus. A Read from CSR 13 is decoded if the Data/Status bit of the command word (bit 1) is set to Status (hi).

Two resets are generated RES and RESP. RES is a generated reset to clear control bistables. It is generated by

(a) Write to CSR 13 Data bits 15 = Hi and 14 = Lo.

(b) Read from CSR 15.

(c) C – R network for power on reset.

(d) END OF STORE signal from Brush Address card.

(e) END OF PICTURE signal from NON-DATA field pulse gated with Picture Sync Detected bistable.

RESP is used to reset the Picture Sync Detected bistable, so is the same as RES except source (e). Bit 0 of the command word is clocked into bistable (IC JA) and becomes a 'GO' signal to start the action as defined by other command word bits. This bistable is reset by RES.

Bit 1 defines whether data from the Digital Bus or Status is read during a processor read.

Bit 2 sets Field or Frame mode for the Decoder card EBO 17482 and Encoder card EBO 17481.

Bit 3 defeats error concealment.

Bit 4 sets a Luminance only mode which can be used for special dumps e.g. stencils.

Bit 5 sets Encoded or Decoded mode. The nominal modes are Decoded for and Encoded NTSC to maintain DLS 6000/1 Library System compatibility.

Bits 6 and 7 define the Digital Link System mode:-

OFF –	Inactive state.
CONVERT –	Enables the Encoder card EBO 17481 and Decoder card EBO 17482 to be used with processor data.
DUMP –	Dumps framestore data in a video format.
LOAD –	Reconverts previously dumped picture into a framestore.

Bits four to seven are decoded by a PROM (IC DA) which produces data routing enable signals and LED drives.

LED 5 Dump is driven when in dump mode. LED 9 LOAD when in Load mode and LED 2 ENCODE if encoded data is used.

CSR = 13

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Reset

Write

1 1 X

Reset a) Write #C000 CSR 13
b) Read CSR 15
c) Power - on

Commands

Write

15	14		7	6	5	4	3	2	1	0
1	0	X	Mode		Encode	Lum Only	Conceal	Frame	Stat	Go

Off	0	0						
Convert	0	1						
Dump	1	0						
Load	1	1						
Decoded			0					
Encoded			1					
Lum & Chr				0				
Lum Only				1				
Conceal Off					0			
Conceal On					1			
Field						0		
Frame						1		
Read Data							0	
Read Status							1	
Set up								0
Go								1

Table 2 Paintbox Digital System

Enable	A	B	C	D	E	F	G	H	J	K			
Data Path to Ser. Bus	Brush Lum to Ser. Bus	Brush Chr Tape Bus/ Ser. Bus	Enable Tape Bus/ Ser. Bus	Direction to Ser. Bus	Deserialiser to Ser. Bus	Conceal RAM to Brush Bus	Ser. Bus to Brush Bus	Decoder to Tape Bus	Encoder to Tape Bus	Processor Bus Data	Brush Bus Data	Tape Bus Data	Serialised Bus Data
Mode IC	AD	BB	AC	AC	DB	EA	BD, CE	Enc.BG,BF	Enc.CB	Enc.AB			
OFF	1	1	1	1	1	1	1	1	1	1	–	–	–
Dump Decoded L+C	01	10	1	1	1	1	1	1	1	1	From Frame Store	–	To Serialiser
Dump Decoded L Only	0	1	1	1	1	1	1	1	1	1		–	
Dump Encoded L+C	1	1	0	0	1	1	1	1	0	1		Encoder	
Dump Encoded L Only	1	1	0	0	1	1	1	1	0	1			
Load Decoded L+C	1	1	1	1	0	1	0	1	1	1	To Frame Store from I/F	–	From Deserialiser or Conceal RAM
Load Decoded L+C Err	1	1	1	1	1	0	0	1	1	1		–	
Load Decoded L Only	1	1	1	1	0	1	0	1	1	1		–	
Load Decoded L Only Err	1	1	1	1	1	0	0	1	1	1		–	
Load Encoded L+C	1	1	0	1	0	1	1	0	1	1	To Frame Store from Decoder	–	
Load Encoded L+C Err	1	1	0	1	1	0	1	0	1	1		Decoder	
Load Encoded L Only	1	1	0	1	0	1	1	0	1	1			
Load Encoded L Only Err	1	1	0	1	1	0	1	0	1	1			
Convert Decode	1	1	1	1	1	1	1	0	1	0	Decoder	Processor	–
Convert Encode	1	1	1	1	1	1	1	1	0	1	Encoder	Processor	–

Notes: (a) Signals a Lo (0) to enable.

(b) During a Dump Decoded L+C enables A and B alternate byte by byte.

17. ADJUSTMENTS

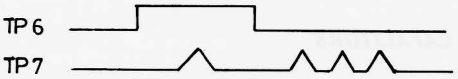
Switch Settings

	ON	OFF	USED FOR
1	NON-CONC	CONCEAL	LOAD
2	TEST	NORMAL	DUMP
3	NOISE DET	NORMAL	LOAD
4	PAL	NTSC	LOAD

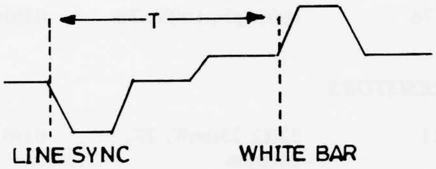
Normal settings PAL 4 on 1, 2, 3, off
NTSC all off.

Switch 1 forces non-conceal, in off position software has control.

VR1 at bottom of card edge. This is used to adjust the position of a window at the beginning of each line during which the positive edge of the white bar is detected during a load. To set this trigger a scope on TP6 and also view TP7. Adjust VR1 to centre the pulse at the start of the line in the window.



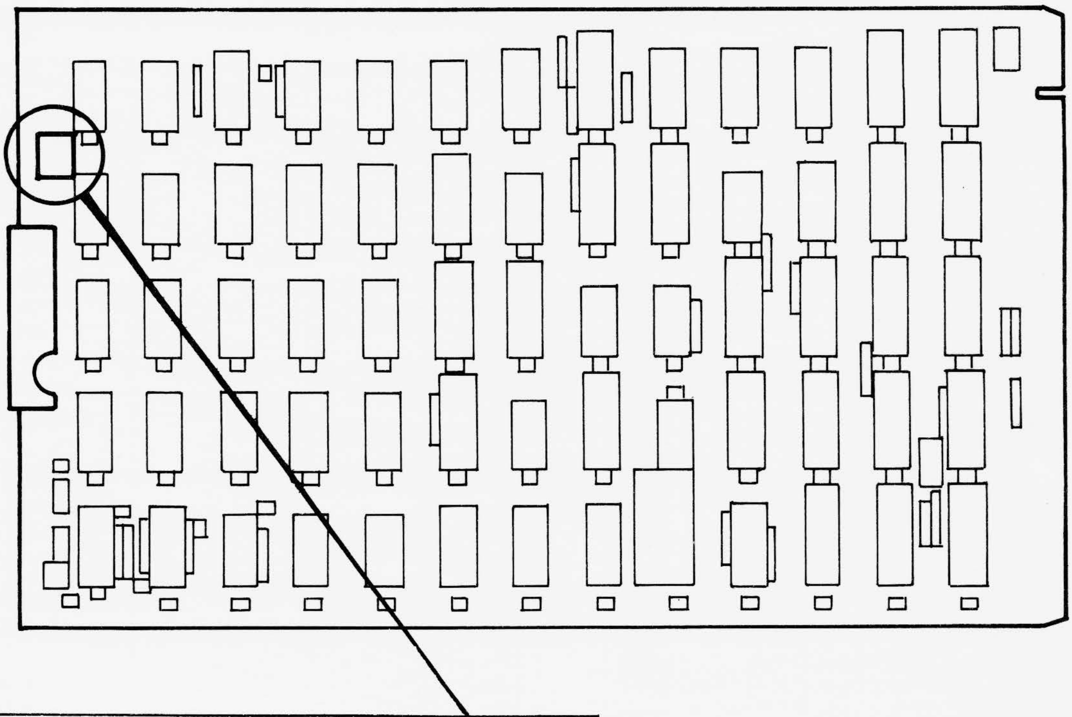
For compatibility of dumped tapes between machines the position of the white bar must be correct with respect to line syncs. This time is determined by monostable KE pin 4.



	T	KE Output Pulse Width	C1
PAL	11.0 – 11.2μS	3.65μs	560 + 33pF
NTSC	10.6 – 11.0μs	2.95μs	470pF

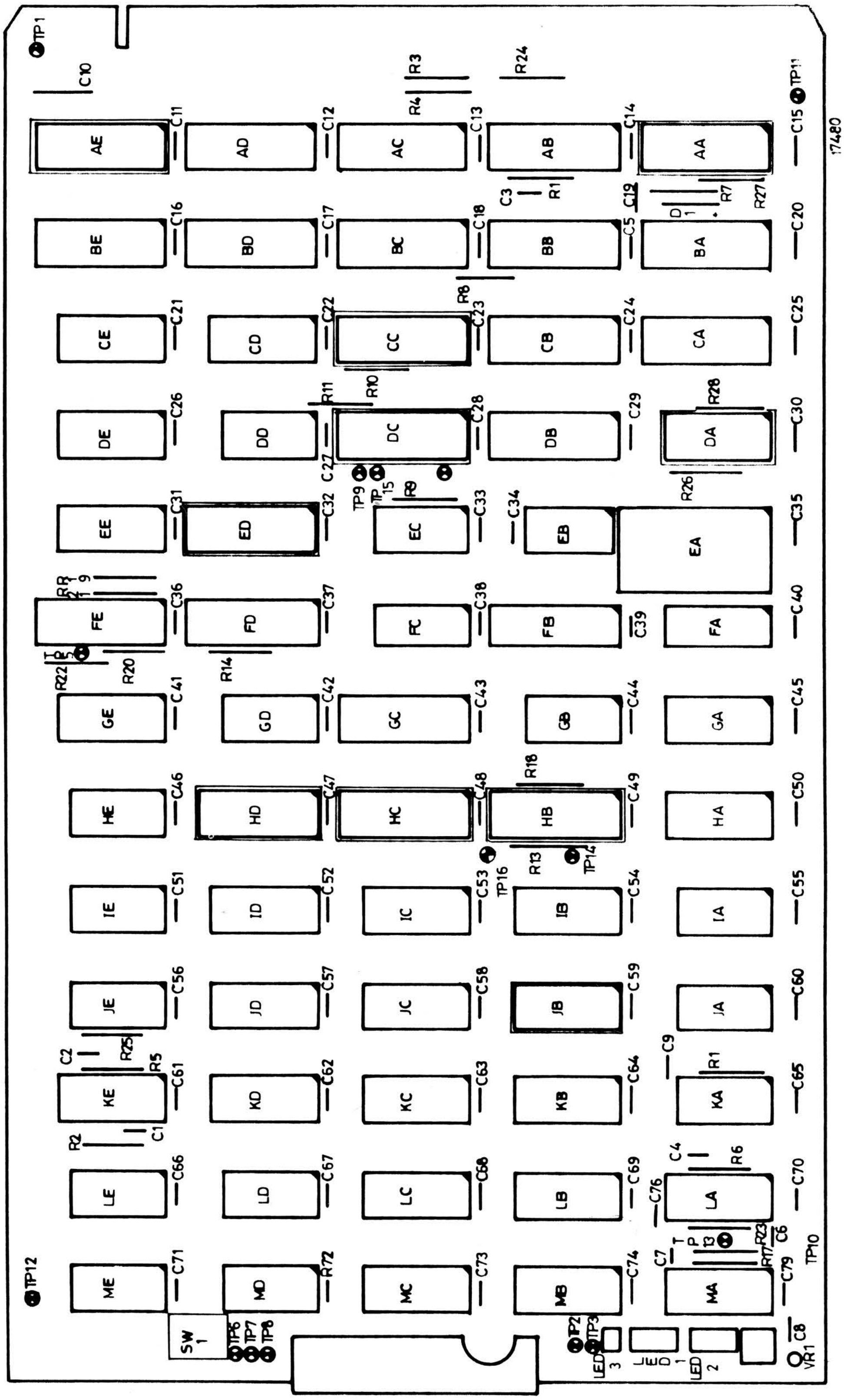
REF.	DESCRIPTION	STOCK CODE
CAPACITORS		
C1	470pF, 100V, 5%	03/06/0438
C2	1500pF, 100V, 10%	03/06/0144
C3	1000pF, 100V, 10%	03/06/0314
C4	220pF, 100V, 10%	03/06/0055
C5	10µF, 35V, 20%	03/03/0199
C6	1500pF, 100V, 10%	03/06/0144
C7	1200pF, 100V, 10%	03/06/050Y
C8	220pF, 100V, 10%	03/06/0055
C9	100pF, 100V, 10%	03/06/0306
C10	NOT FITTED	
C11-C75	100000pF, 50V, +80%-20%	03/06/0233
C76	10000pF, 100V, 2%	03/06/0918
RESISTORS		
R1	220Ω, 250mW, 2%, 100ppm	01/01/0441
R2	9.1kΩ, 250mW, 2%, 100ppm	01/01/093X
R3, R4	220Ω, 250mW, 2%, 100ppm	01/01/0441
R5-R7	10kΩ, 250mW, 2%, 100ppm	01/01/0948
R8, R9	560Ω, 250mW, 2%, 100ppm	01/01/0581
R10	4.7kΩ, 250mW, 2%, 100ppm	01/01/084Y
R11	10kΩ, 250mW, 2%, 100ppm	01/01/0948
R12	NOT FITTED	
R13	4.7kΩ, 250mW, 2%, 100ppm	01/01/084Y
R14	220Ω, 250mW, 2%, 100ppm	01/01/0441
R15	470Ω, 250mW, 2%, 100ppm	01/01/0557
R16	11kΩ, 250mW, 2%, 100ppm	01/01/0956
R17, R18	10kΩ, 250mW, 2%, 100ppm	01/01/0948
R19, R20	560Ω, 250mW, 2%, 100ppm	01/01/0581
R21, R22	4.7kΩ, 250mW, 2%, 100ppm	01/01/084Y
R23	10kΩ, 250mW, 2%, 100ppm	01/01/0948
R24	220Ω, 250mW, 2%, 100ppm	01/01/0441
R25-R28	560Ω, 250mW, 2%, 100ppm	01/01/0581
VR1	5kΩ, 50mW, 10%	02/04/0069
INTEGRATED CIRCUITS		
AA	16L8-ACN	04/01/779X
AB	74LS244N	04/01/2828
AC	74LS245N	04/01/3824
AD	74LS373N	04/01/3921
AE	7649A-5	04/01/5258
BA	74LS244N	04/01/2828
BB	74LS373N	04/01/3921
BC	74LS244N	04/01/2828
REF.	DESCRIPTION	STOCK CODE
INTEGRATED CIRCUITS (Cont.)		
BD	74LS373N	04/01/3921
BE	74S374N	04/01/4294
CA	74LS273N	04/01/3115
CB	74LS373N	04/01/3921
CC	16L8-ACN	04/01/779X
CD	74LS166N	04/01/318Y
CE	74S161N	04/01/5231
DA	82S123N	04/01/7099
DB	74LS374N	04/01/3328
DC	16L8-ACN	04/01/779X
DD	74LS280N	04/01/670X
DE	74S161N	04/01/5231
EA	6116P-3	04/03/345Y
EB	74LS30N	04/01/0469
EC	74LS74N	04/01/0728
ED	16L8-ACN	04/01/779X
EE	74S161N	04/01/5231
FA	74LS163N	04/01/1317
FB	74LS374N	04/01/3328
FC	74LS164N	04/01/3719
FD, FE	16L8-ACN	04/01/779X
GA	74LS163N	04/01/1317
GB	74LS280N	04/01/670X
GC	74S374N	04/01/4294
GD	74LS164N	04/01/3719
GE	74LS175N	04/01/1457
HA	74LS163N	04/01/1317
HB	16L8-ACN	04/01/779X
HC	7649A-5	04/01/5258
HD	27S185PC	04/01/8397
HE	74LS164N	04/01/3719
IA	74LS00N	04/01/006X
IB	74LS175N	04/01/1457
IC	74S161N	04/01/5231
ID	74LS161N	04/01/1287
IE	74LS00N	04/01/006X
JA	74LS74N	04/01/4294
JB	NOT FITTED	
JC	74S161N	04/01/5231
JD	74LS161N	04/01/1287
JE, KA	74LS74N	04/01/4294
KB	74LS161N	04/01/1287
KC	74S161N	04/01/5231
KD	74LS161N	04/01/1287
KE	74221N	04/01/157Y
LA	74LS221N	04/01/1589
LB	74LS161N	04/01/5231
LC	74LS191N	04/01/1511
LD	74LS164N	04/01/3719
LE	74LS74N	04/01/4294
MA	74LS221N	04/01/1589
MB	74LS161N	04/01/5231
MC	74LS191N	04/01/1511
MD	74S00N	04/01/0035
ME	74LS08N	04/01/417Y
MISCELLANEOUS		
LED1, 2	Light emitting diode Red	06/03/0041
LED3	Light emitting diode Green	06/03/0327
SW1	Dil Switch 4W	26/06/0176
D1	Diode 75V	06/01/0083

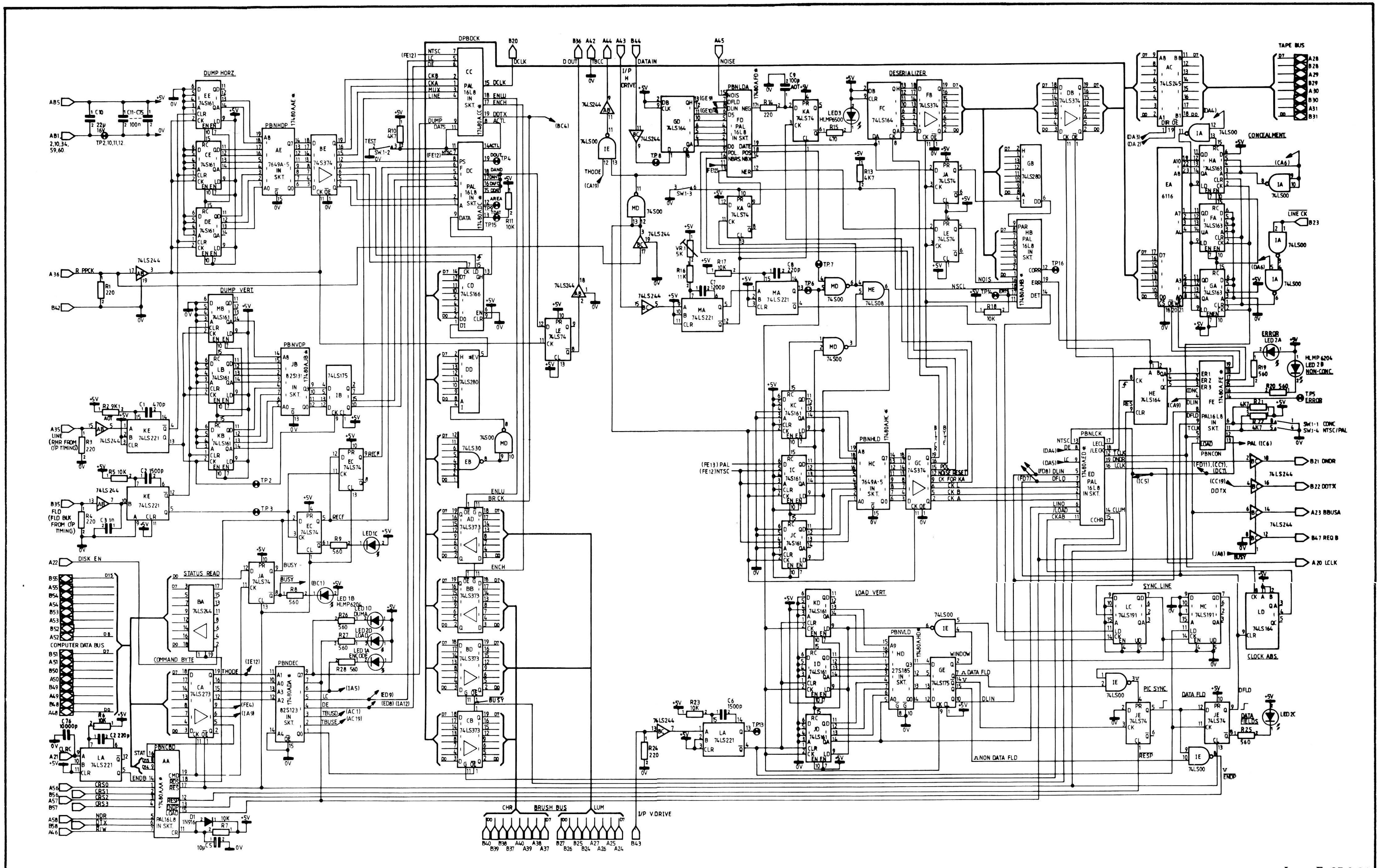
17480 Component List



	1	2	3	4
NON CONCEALMENT	ON			
CONCEALMENT ON	OFF			
ENGINEERING TEST ONLY				
DUMPING		ON		
NOISE DETECTION				
LOAD			ON	
7000				OFF
7001				ON
NORMAL CONFIGURATION				
7000	OFF	OFF	OFF	OFF
7001	OFF	OFF	OFF	ON

17480, Figure 1 Digital Interface Card Switch Configurations


TP1
C10
R3
R24
R4
TP11
17480
AE
C11
AD
C12
AC
C13
AB
C14
AA
C15
C3
R1
C19
D1
R7
R27
BE
C16
BD
C17
BC
C18
BB
C5
BA
C20
R8
CE
C21
CD
C22
CC
C23
CB
C24
CA
C25
R11
R10
R28
DE
C26
DD
DC
C28
DB
C29
DA
C30
C27
TP9
TP15
R9
R26
EE
C31
ED
C32
EC
C33
C34
EB
EA
C35
R21
R19
FE
C36
FD
C37
FC
C38
FB
C39
FA
C40
TP5
R22
R20
R14
GE
C41
GD
C42
GC
C43
GB
C44
GA
C45
R18
HE
C46
HD
C47
HC
C48
HB
C49
HA
C50
TP16
R13
TP14
IE
C51
ID
C52
IC
C53
IB
C54
IA
C55
JE
C56
JD
C57
JC
C58
JB
C59
JA
C60
C2
R25
R5
C9
R1
KE
C61
KD
C62
KC
C63
KB
C64
KA
C65
R2
C1
C4
R6
LE
C66
LD
C67
LC
C68
LB
C69
C76
LA
C70
TP12
TP13
R23
C6
R17
TP10
ME
C71
MD
R72
MC
C73
MB
C74
C7
MA
C79
SW 1
TP6
TP7
TP8
TP2
TP3
LED 3
LED 1
LED 2
C8
VR1



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17480, Figure 2 Digital Interface Card : Circuit Diagram and Component Layout

ENCODER CARD

17481

1. GENERAL

The Encoder card takes picture data in its component luminance and chrominance form and arithmetically generates an NTSC encoded output.

Encoded data is used to maintain compatibility between the DPB 7000/1 Paintbox and DLS 6000 Library System.

Data conversion circuit also level - change the video data to maintain compatibility. The Encoder card contains reverse data conversion circuits to level - change the Decoder card EBO 17482 output.

A clock generation circuit for the Decoder is also incorporated on the Encoder card.

Processor bus decode and data latches set the Encoder mode and data paths.

2. ENCODER CIRCUIT

Data in its component luminance (Y) and chrominance (U - V) form from the brush bus is level - changed in two PROM look-up tables one for luminance (IC AE) and the other for chrominance (IC AD). Brush Bus data alternates between Y – U and Y – V, so a U – V signal controls which look-up table is used within the chrominance PROM.

Since the picture data sample rate is 4 x colour sub-carrier (4fsc) a simple arithmetic operation can generate an encoded data stream.

Along a picture line a four step sequence encodes the data:-

	1	2	3	4
Output	Y + U	Y + V	Y – U	Y – V
Brush Bus Input Lum.	Y	Y	Y	Y
Chrominance	U	V	U	V

An eight-bit adder - subtractor (ICs BD, BE and BF) and over/under flow correction circuits (IC CD and CE) are controlled by a 2-bit pixel counter and a 2-bit line counter.

To encode picture data correctly into NTSC form the four step sequence changes phase in the following line related way, depending on whether the picture is a Field or a Frame:

		1	2	3	4
Frame	Line n	Y + U	Y + V	Y – U	Y – V
	n + 1	Y + U	Y + V	Y – U	Y – V
	n + 2	Y – U	Y – V	Y + U	Y + V
	n + 3	Y – U	Y – V	Y + U	Y + V

The pixel counters (IC DG) is incremented by a Picture Point Clock (PPCK) signal, and the line counter (IC DE) by a Line Clock signal, from the Brush Address card. A field/frame multiplexer (IC) and exclusive OR gates (IC DD) control the add/subtract function.

Encoder output data can be gated (IC AC) onto a Digital Bus and subsequently processed by the Digital Interface card EBO 17480.

A simple resistor digital to analogue converter (IC CC) on the Digital Bus is used to monitor the encoder circuit output when testing.

3. PROCESSOR DECODE

Processor commands are decoded by a PAL (IC AA), which generates enable signals and strobe pulses as seen in the table below.

To enable the processor to read data from the digital bus RDA enables a buffer (IC BB). Data from processor to digital bus is clocked into register (IC AB).

Digital Link System commands are clocked into a register (IC CA) the outputs of which are used to control the Encoder card mode.

RDA	Read Data	CSR 13	Read		
WDA	Write Data	CSR 13	Write	D15 = 0	D14 = 0
COM	Write Command	CSR 13	Write	D15 = 1	D14 = 0
RES	Reset or or	CSR 13 CSR 15	Write Read Power-on CR network	D15 = 1	D14 = 1

Encoder Card Enable Signals and Strobe Pulses

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	X	X	X	X	X	X	Mode		Encode	Lum Only	Conceal	Frame	Stat	Go
												*			*

	7	6	5	4	3	2	1	0
OFF	0	0						
CONVERT	0	1						
DUMP		1	0					
LOAD		1	1					
DECODED DATA				0				
ENCODED DATA				1				
LUM + CHROM					0			
LUM ONLY					1			
CONCEAL OFF						0		
CONCEAL ON						1		
FIELD							0	
FRAME							1	
READ DATA								0
READ STATUS								1
SET-UP								0
GO								1

* Not used in Encoder card EBO 17481

How a Command Word is Constructed

This command word is constructed as follows:

Bit 1 STAT/DATA is used to enable RDA signal.

Bit 2 FIELD/FRAME controls encoder line sequence.

Bits 4-7 are decoded by a PROM (IC DA) which generates data routing signals and LED drives:

(a) Decoder conversion PROMs to Brush Bus (enables ICs BF and BG LED 4).

(b) Processor to Digital Bus (enables IC AB).

(c) Encoder output to Digital Bus (enables IC AC LED 3).

(d) Encoder busy LED 1.

(e) Convert mode LED 2.

Bits 6 and 7 mode also control the clock control circuit.

4. CLOCK CONTROL

A programmed PAL (IC BA) performs two functions:-

(a) Clock source multiplexer.

(b) Picture Point to Bit Clock multiplier.

Depending on the Mode (command word bits 6 and 7) the appropriate source of Picture Point Clock is selected:-

D7	D6			
1	0	Dump Clock	DCLK	from Digital Interface EBO 17480
1	1	Load Clock	LCLK	
0	X	Convert Clock	CCLK	from WDA Write Data from processor.

During a LOAD operation the Decoder card EBO 17482 requires 8-bit clocks for each picture point. Within the PAL a 4-bit counter and start-stop logic generate a stream of eight pulses for each picture point clock. Bit clocks are generated from a 4fsc signal.

5. DECODE CONVERSION

The Decoder card EBO 17482 output needs to be level translated for use within the DPB 7000/1 Paintbox. Luminance and chrominance look-up tables (PROMs IC AG and AF) are used (the reverse of those used during encoding) prior to bus buffers (ICs BF and BG) to enable data onto the Brush Bus.

6. ADJUSTMENTS

Switch Settings

SWITCH	ON	OFF	USED FOR
1	NON-CONC	CONCEAL	LOAD
2	TEST	NORMAL	DUMP
3	NOISE DET	NORMAL	LOAD
4	PAL	NTSC	LOAD

Normal settings: SW1-3 OFF, SW4 ON for PAL, OFF for NTSC.

Switch 1 on forces non-conceal, in off position software has control.

VR1 at bottom of card edge. This is used to adjust the position of a window at the beginning of each line during which the positive edge of the white bar is detected during a load. To set this trigger a scope on TP6 and also view TP7. Adjust VR1 to centre the pulse at start of line in the window.

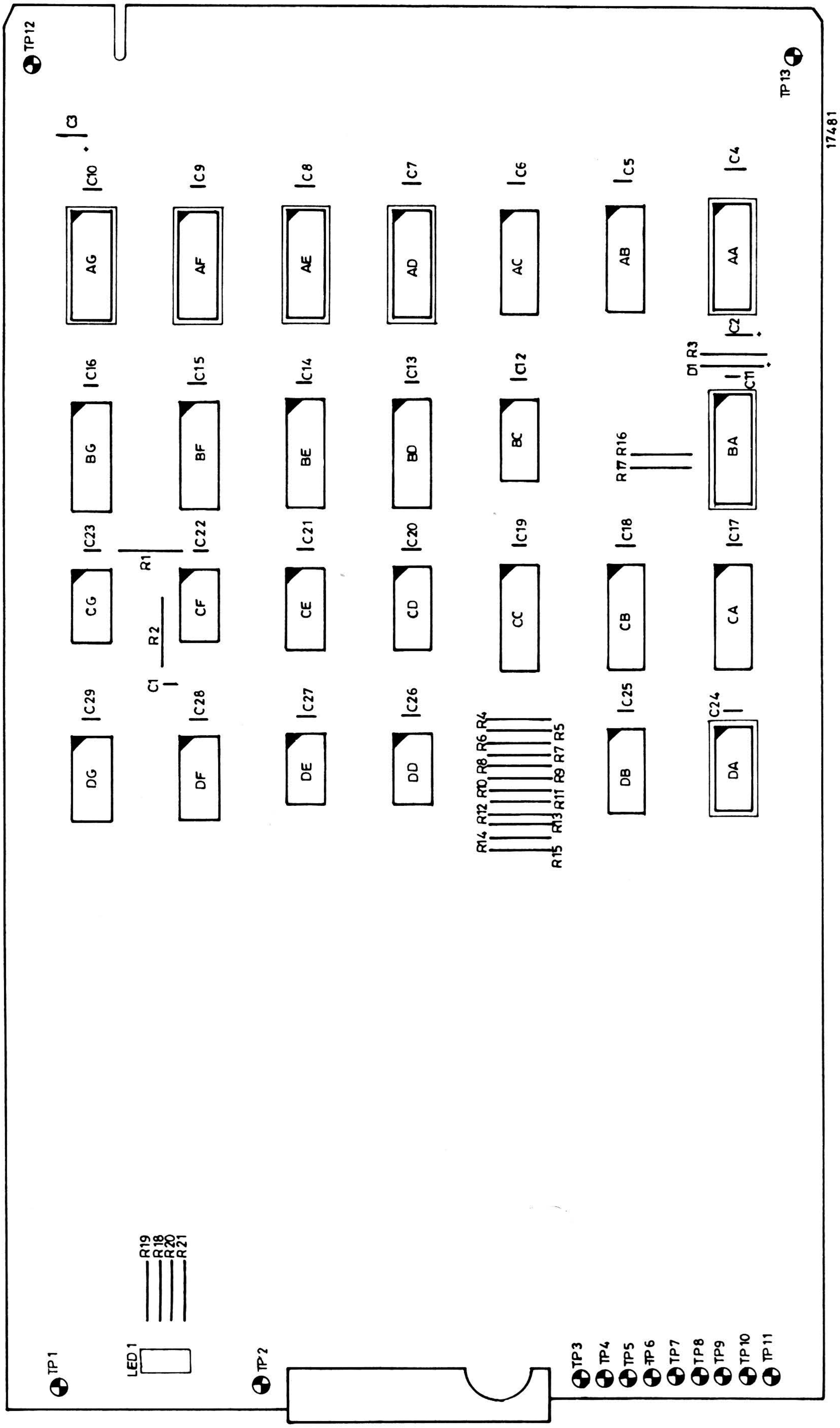
For compatibility of dumped tapes between machines the position of the white bar must be correct with respect to line syncs. This time is determined by monostable KE pin 4.

	T	KE Output Pulse Width	C1
PAL	11.0 – 11.2µs	3.65µs	560 + 33pF
NTSC	10.6 – 11.0µs	2.95µs	470pF

REF.	DESCRIPTION	STOCK CODE
CAPACITORS		
C1	100pF, 100V, 20%	03/05/0386
C2	10μF, 16V, 20%	03/03/0172
C3	22μF, 16V, 20%	03/03/0253
C4-C29	100000pF, 50V, +80% −20%	03/06/0233
RESISTORS		
R1	10kΩ, 250mW, 2%, 100ppm	01/01/0948
R2	220Ω, 250mW, 2%, 100ppm	01/01/0441
R3	10kΩ, 250mW, 2%, 100ppm	01/01/0948
R4	1kΩ, 250mW, 2%, 100ppm	01/01/0646
R5	2kΩ, 250mW, 2%, 100ppm	01/01/0719
R6,R7	4kΩ, 250mW, 2%, 100ppm	01/01/0816
R8,R9	16kΩ, 250mW, 2%, 100ppm	01/01/098Y
R10	56kΩ, 250mW, 2%, 100ppm	01/01/112X
R11	120kΩ, 250mW, 2%, 100ppm	01/01/117Y
R12	4kΩ, 250mW, 2%, 100ppm	01/01/0816
R13	16kΩ, 250mW, 2%, 100ppm	01/01/098Y
R14,R15	8.2kΩ, 250mW, 2%, 100ppm	01/01/0921
R16,R17	10kΩ, 250mW, 2%, 100ppm	01/01/0948
R18-R21	560Ω, 250mW, 2%, 100ppm	01/01/0581

REF.	DESCRIPTION	STOCK CODE
SEMICONDUCTORS		
D1	Diode, IN916, 75V, 500M	06/01/0083
INTEGRATED CIRCUITS		
AB	74LS74N	04/01/3328
AC	74LS244N	04/01/2828
BC	74S182N	04/01/3735
BD,BE	74S381N	04/01/4308
BF,BG	74LS244N	04/01/2828
CA	74LS273N	04/01/3115
CB,CC	74LS244N	04/01/2828
CD,CE	74LS157N	04/01/1236
CF	74LS132N	04/01/3158
CG	74LS08N	04/01/417Y
DB	74LS153N	04/01/118X
DD	74LS86N	04/01/0833
DE	74LS04N	04/01/0191
DF	74LS109N	04/01/3166
DG	74LS161N	04/01/1287
AA,AD,AE AF,AG,BA DA	Programmed Set Make From 1 x 04/01/541X 16L8 2 x 04/01/5258 7649A-5 2 x 04/01/3107 6309-1N 1 x 04/01/6629 16R6 1 x 04/01/2313 74S288	
MISCELLANEOUS		
LED 1	Light Emitting Diode 1.6V, Red	06/03/0041

17481 Component List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17481
C3
C10
C9
C8
C7
C6
C5
C4
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AE
AD
AC
AB
AA
C2
D1 R3
C11
C16
C15
C14
C13
C12
BG
BF
BE
BD
BC
R17 R16
BA
C23
R1
C22
C21
C20
C19
C18
C17
CG
CF
CE
CD
CC
CB
CA
R2
C1
C29
C28
C27
C26
C25
C24
R4 R6 R8 R10 R12 R14
R5 R7 R9 R11 R13 R15
DG
DF
DE
DD
DB
DA
R19
R18
R20
R21
LED 1
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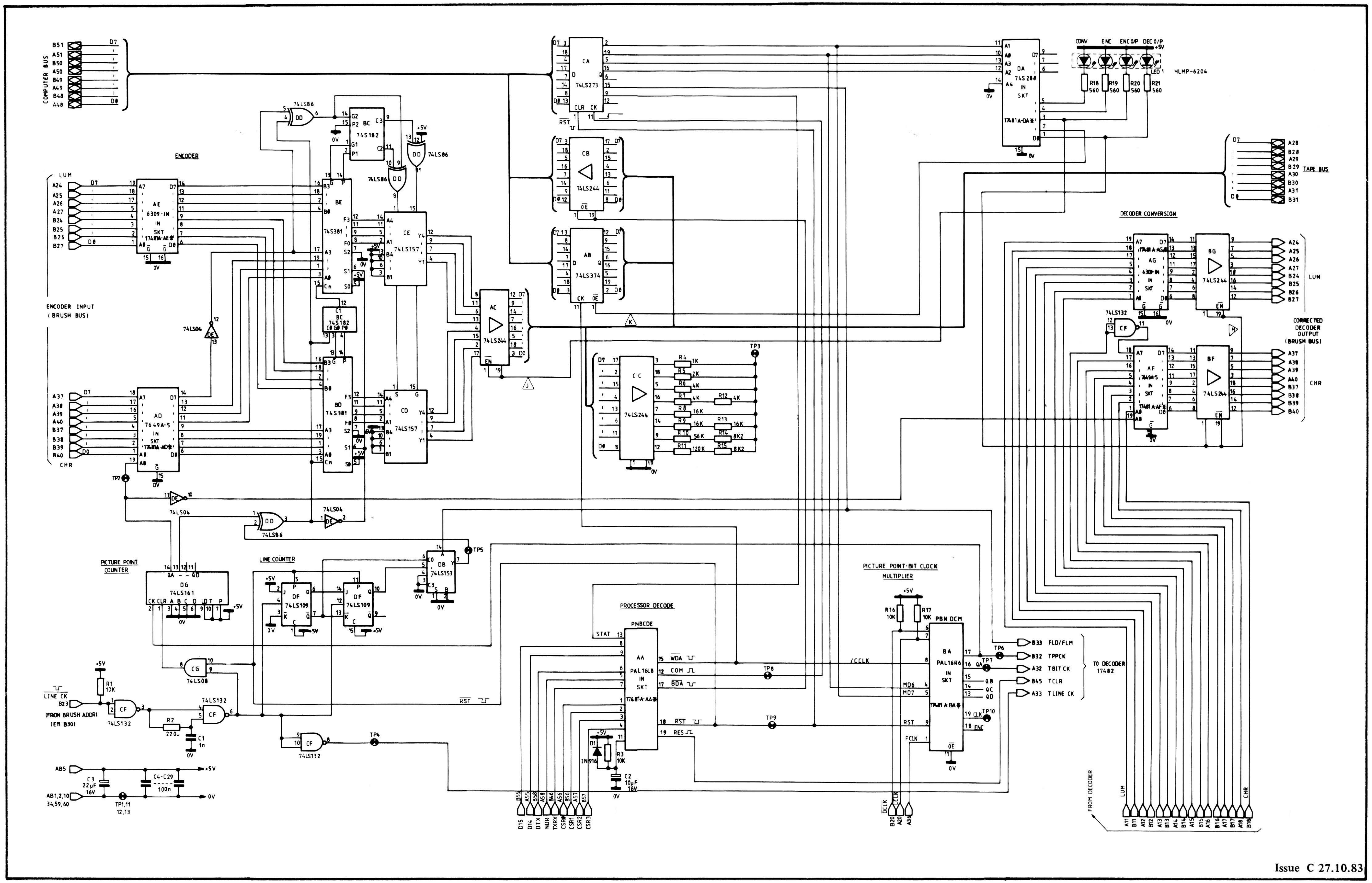
TP2
TP3
TP4
TP5
TP6
TP7
TP8
TP9
TP10
TP11



Issue C 27.10.83

17481, Figure 1 Encoder Card : Circuit Diagram and Component Layout

DECODER CARD

17482

1. INTRODUCTION

The purpose of this card is to take encoded video data as it comes from the digital link system and separate it into luminance and (demodulated) chrominance components. It should be appreciated that the card works at digital data rate therefore references to things such as 'oneline delay' do not mean a real time delay of one line, but a delay such that input and output values are sampled from consecutive lines.

2. CIRCUIT DESCRIPTION

The principles of operation are best understood by reference to the simplified block diagram.

In the band pass filter, an average between two data values separated by four picture points (A and C) is calculated, and then the data value midway between the two (B) is subtracted from the result. Subcarrier components are in phase between A and C, but 180°C different at B. The result is that at D, d.c. components are totally cancelled, whilst the subcarrier components are present at full amplitude; at other frequencies, partial cancellation will have occurred. Thus we have a band pass filter (with gradual cut off), centred around the subcarrier. Only frequency components within this pass band will be used in the subsequent vertical comb filter for separating chrominance.

Registers BA, CA, DA and EA provide the four picture point of delay, point A being the input to BA and point C being the output of EA. The average between A and C is clocked into register CB; therefore the intermediate point B is taken not from the output of CA but from the output of DA, so that there is a corresponding picture point of delay. DA and EA are both inverting registers. The output of DA is therefore bit-inverted (as is required for DB and EB to act as a subtractor), whilst the output of EA is back to normal polarity. The output of the subtractor is clocked into register FB to provide the output D. It should be noted that data at D has undergone four clocks of delay, whilst that at C has undergone four clocks of delay; subcarrier components at these points are therefore 180° out of phase with each other.

In the combiner filter, an average between two data values separated by two lines (D and F) is calculated and the output is subtracted from the data value midway between the two (E). As subcarrier components alternate in phase from one line to the next, at the output of G these will present unattenuated, whilst other components will have been cancelled. It remains only to demodulate the signal at G to obtain the chrominance output.

In principle, the luminance output is obtained by subtracting the signal at G from the original signal. However, the signal at G has undergone a one line delay from point D; we therefore need a corresponding one line delay from C to H. As was noted earlier the subcarrier components at points C and D are 180° out of phase with each other, and therefore effective subcarrier removal is obtained by adding the signal at G to that at H.

The above description has assumed a field mode picture, that is field one followed by field two as for normal video. In frame mode, the picture is de-interleaved, that is consecutive lines are from alternate fields. Hence, to decode in the same fashion as described, each of the one line delays must be replaced by a two line delay, so that consecutive lines of the same field at used in the manipulation as before. Field or frame mode is controlled by a signal on pin B33, from the Encoder card EBO 17481.

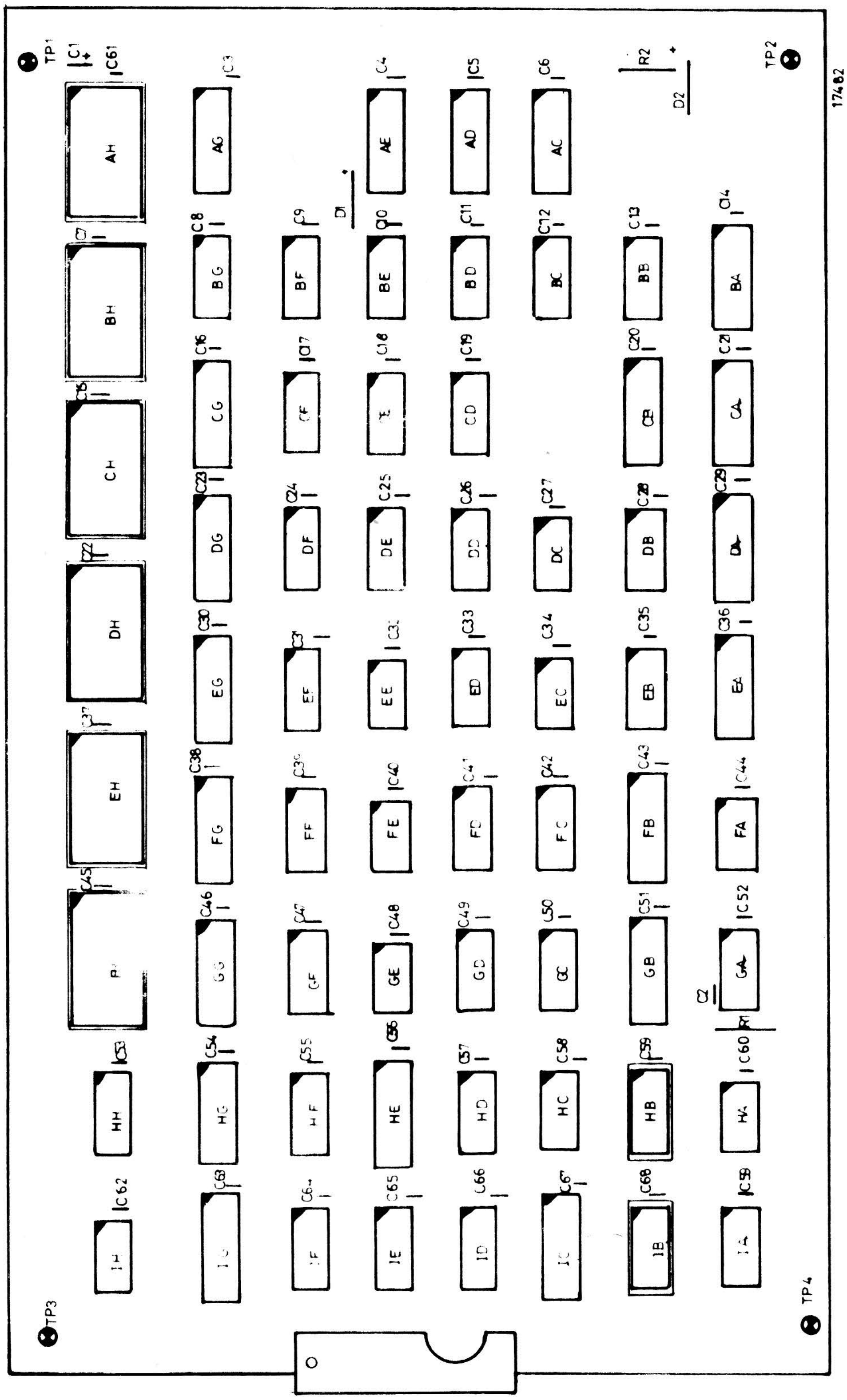
We are now in a position to relate this to the circuit diagram. Counter ID, IE and IF are reset to zero each line counts picture points along the line, so generating addresses for CH, DH, EH, FH, AH, and BH, which each provide one line of delay. This is accomplished under the control of signals from ROM IB driven by counter IA, such that for each picture point the old data value (from one line ago) is clocked from the RAM into the subsequent register during the first part of the cycle, and the new data value is written from the preceeding register into the RAM during the latter part of the cycle. The data selectors EF, FF, GF, HF, CF and DF switch between field and frame modes.

Thus, in field mode, CH is the delay between points D and E (of the block diagram) DH is that between E and F, and BH is that between C and H. In frame mode, CH and DH are between D and E, EH and FH are between E and F, and BH and AH are between C and H. Data between points D and F is averaged in adder GC, GD and part of GE, and subtracted from that at point E in subtractor GB, FC, FD and part of FE. The demodulator comprises DC, EC, CD and BD using digital rate 'subcarrier' made by dividing digital picture point clock by four in HA. The phase of this 'subcarrier' is alternated line by line (for field mode) or after each two lines (for frame mode) by the appropriate signal from IH as selected by HH. The addition of signals at points G and H is accomplished by adder DE, CE, and BE, whose output is limited to the range zero to 255 by BF and BG to provide the luminance output.

The combiner filter works effectively only if there is no substantial difference in data over the two lines of interest, that is between D and F. To avoid any possibility of significant residual subcarrier effects, it is possible to modify the operation of the decoder if this condition is not satisfied. To this end, the difference between data at D and F is found by subtractor HE, HD, HC and part of GE. This is used to address PROM HB whose output is high unless the difference exceeds a predetermined level, when the selectors ED and DD will no longer pass the subcarrier component at point G but will pass the data from point E. In this case, the luminance output will consist of the difference between the card input signal and the output of the band pass filter, that is with all components in the wide notch centred on subcarrier removed. This ensures that no chrominance is present on the luminance output, at the expense of having removed some of the luminance components in the chrominance passband.

REF.	DESCRIPTION	STOCK CODE
CAPACITORS		
C1	22µF, 16V, 20%	03/03/0253
C2	39pF, 100V, 10%	03/06/0039
C3-C69	100000pF, 50V, +80% −20%	03/06/0233
RESISTORS		
R1	2.7kΩ, 250mW, 2%, 100ppm	01/01/0734
R2	330kΩ, 250mW, 2%, 100ppm	01/01/1723
SEMICONDUCTORS		
D1,D2	TA 50822800, 70V	06/01/0059
SEMICONDUCTORS		
D1,D2	TA 50822800, 70V	06/01/0059
INTEGRATED CIRCUITS		
AC,AD	74LS244N	04/01/2828
AE-BA	74LS374N	04/01/3328
BB-BE	74LS283N	04/01/3131
BF,BG	74LS157N	04/01/1236
BH	MOS 4801AJ-2	04/03/404X
CA,CB	74LS374N	04/01/3329
CD,CE	74LS283	04/01/3131
CF	74LS157N	04/01/1236
CG	74LS374N	04/01/3328
CH	MOS 4801AJ-2	04/03/404X
DA	74LS534J	04/01/5126
DB	74LS283N	04/01/3131
DC	74LS86N	04/01/0833
DD	74LS157N	04/01/1236
DE	74LS283N	04/01/3131
INTEGRATED CIRCUITS (Cont)		
DF	74LS157	04/01/1236
DG	74LS374N	04/01/3328
DH	MOS 4801AJ-2	04/03/404x
EA	74lS534J	04/01/5126
EB	74LS283N	04/01/3131
EC	74LS86N	04/01/0833
ED,EF	74LS157N	04/01/1236
FA	7404N	04/01/0159
FB	74LS374N	04/01/3328
FC,FD	74LS283N	04/01/3131
FE	74LS86N	04/01/0833
FF	74LS283N	04/0163131
FG	74LS374N	04/01/3328
GA	74LS221N	04/01/1589
GB	74LS240N	04/01/2879
GC,GD	74LS283N	04601/3131
GE	74LS86n	04/01/0833
GF	74LS157N	04/01/1236
GG	74LS374N	04/01/3328
HA	74LS74N	04/01/0728
HB	Prom Set Make From 1 Off (04/01/2313) 74S288N 1 Off (04/01/2305) 7611A-5	
HC,HD	74LS283N	04/01/3131
HE	74LS240N	04/01/2879
HF	74LS157N	04/01/1236
HG	74LS374N	04/01/3328
HH	74LS157N	04/01/1236
IA	74S161N	04/01/5231
IB	Prom Set Make From 1 Off (04/01/2305) 74S288N 1 Off (04/01/2305) 7611A-5	
IC	74LS374N	04/01/3328
ID,IE	74LS161N	04/01/1287
IF	74LS161N	04/01/1287
IG	74LS240N	04/01/2879
IH	74LS74N	04/01/0728

17482 Component List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C1
C61
C3
C4
C5
C6
R2
D2
TP2
17482
AH
AG
D1
AE
AD
AC
C7
C8
C9
C10
C11
C12
C13
C14
BH
BG
BF
BE
BD
BC
BB
BA
C15
C16
C17
C18
C19
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C21
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CG
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CE
CD
CB
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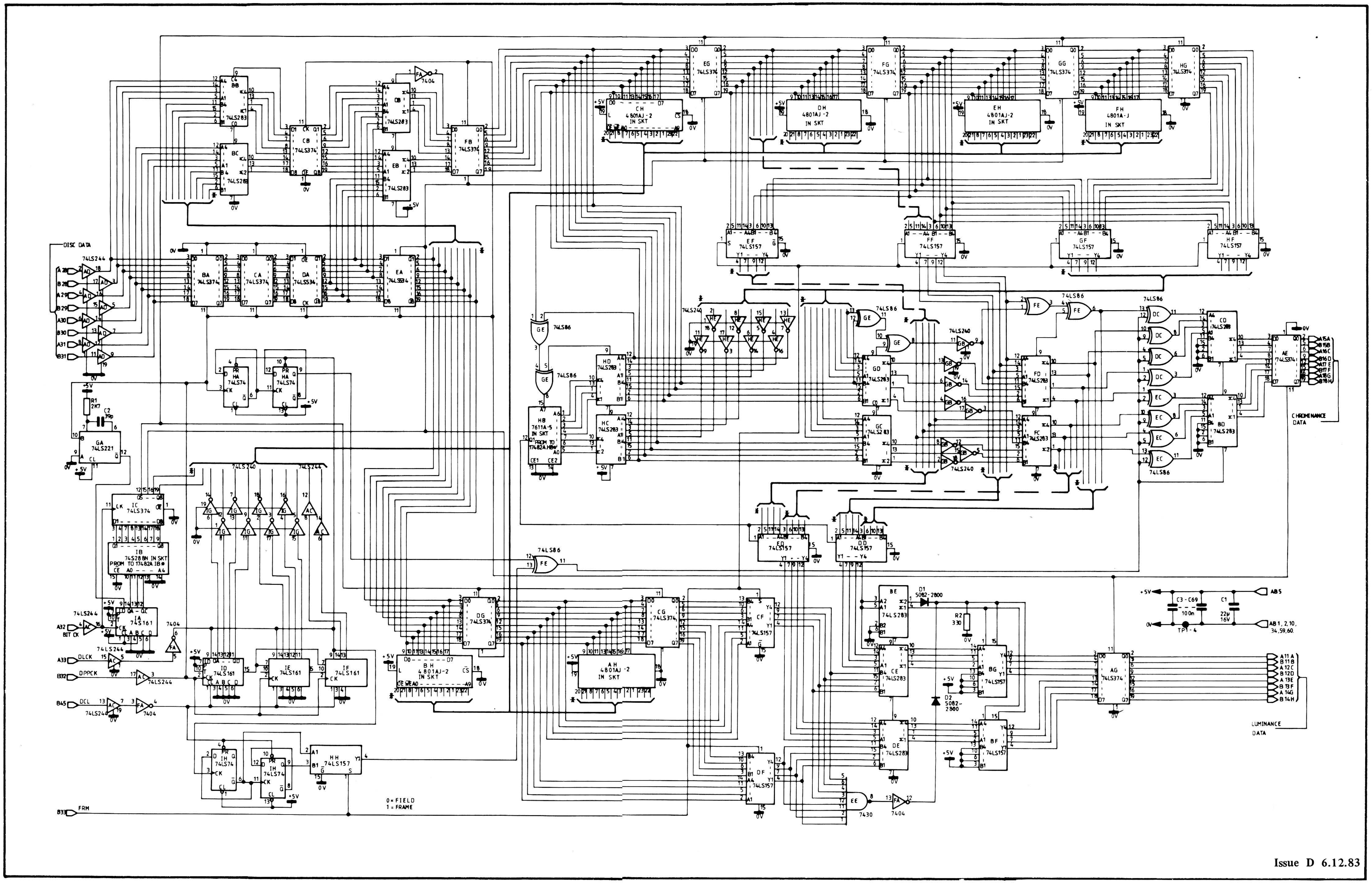


Issue D 6.12.83

17482, Figure 1 Decoder Card : Circuit Diagram and Component Layout

DIGITAL INTERFACE SYSTEM

1. GENERAL

The Digital Interface System for the DPB 7000/1 Digital Paintbox enables disk stored pictures to be transferred from disc along a standard video link in a digitally encoded form and subsequently reloaded maintaining digital integrity. Since information output is in standard video format the system may be used to transfer pictures between machines. Pictures may also be transferred to or from the DLS 6000/1 Digital Library System.

Depending on the video standard, the following cards are required for the Digital Link System.

7000 NTSC

Digital Interface	EBO 17480	Slot E6
Encoder	EBO 17481	Slot E5
Decoder	EBO 17482	Slot E4
New Input Locking	EBO 17564	

7001 PAL

Digital Interface	EBO 17480	Slot E6
New Input Locking	EBO 17564	

The Digital Interface EBO 17480 is designed to be dual-standard, with just PROM changes being required to select NTSC or PAL. Where the circuit description differs, that relating to PAL is in square brackets [] .

DPB 7000 (NTSC) transfers picture data in an encoded (composite) form, where as in DPB 7001 (PAL) data transfer is decoded (Y, U, V).

The Digital Interface (EBO 17480) contains control logic, data formatting and data recovery circuits. Serialised picture data is output in video format via output drivers on the Output Locking card EBO 17449. Input data is digitised on the Input Locking card EBO 17564 by an adaptive slicer and retimed by a special time base corrector.

Pictures are transferred to or from a digital framestore. To do this the Digital Interface controls the Brush Address card.

2. INSTALLATION IN EARLY MACHINES

A number of wiring changes are required on the rear highway of machines built before the digital interface was developed. Access to the highway requires removal of the power supply and also the rear facing SMD highway so the wiring should first be checked using extender cards and a continuity checker or resistance meter. If wiring is necessary it is recommended that the machine be returned to the factory.

The wiring changes are as follows:

(a) Remove wires

E15-A16	to	E6-A43
E15-A17	to	E6-B43
E15-B17	to	E6-A44
E15-B10	to	E6-A42

(b) Replace by KYNAR wires

TLINE	E36-A52	to	E6-A43
VDRIVE	E36-A26	to	E6-B43
TBC CLK	E36-A58	to	E6-A44
GND	E36-A57	to	E6-A42
TBC NOISE	E36-A54	to	E6-A45
GND	E36-A53	to	E6-A42

The wires should run from E36 along the bottom of the lower highway and then upwards to E6.

DISCEN E11-A43 to E10-A43

(c) Check that the following wires exist:

E9-A28	to	E6-A24
A29		A25
A30		A26
A31		A27
E9-B28	to	E6-B24
B29		B25
B30		B26
B31		B27

E9-A37	to	E6-A37	E9-B37	to	E6-B37
A38		A38	B38		B38
A39		A39	B39		B39
A40		A40	B40		B40

Modifications are required on A issue versions of the Brush Address and Size cards:

On issue A Brush Address 17419A add wire

Pin 16 of AB to Edge A43

The circuit shown in Figure 1 is required on the Size card. Issue A cards 17428A require the addition of an extra device (IC1) 74LS240 near to the edge connector. Issue C cards are correct.

Finally the Input Locking card 17412 must be replaced by a new card 17564 which has a time base corrector added to it. The old card 17412 may be retained as a spare for live video but will not work for digital transfers.

3. HOW TO USE THE DIGITAL INTERFACE

For DUMP connect DIGITAL output to input of VTR or DIGITAL input of another Paintbox or slide store. When using the interface for the first time view this output by looking through a monitor.

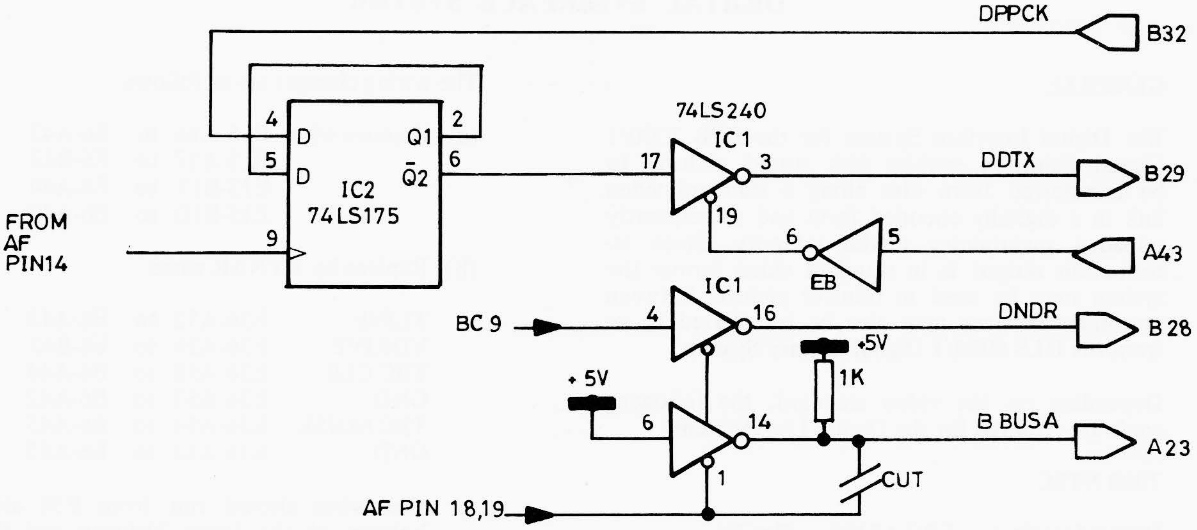


Figure 1 Modifications to 17428 Issue A Cards

For LOAD connect DIGITAL input to output of VTR or DIGITAL output of another machine. Although the digital input of the Paintbox has a time base corrector for data the input syncs must be sufficiently free of jitter for the sync separator or input locking to work properly. This will probably require the use of a time base corrector when loading from VTR.

To DUMP pictures press LIBRARY, DUMP, PICTURE (or CUTOUT), add optional keyword or title if dump is to be selective or CLEAR to dump all. Start VTR or set receiving machine to load. Press END. A message appears on the screen.

"Dumping picture : title"

Each picture takes four seconds to be transferred. A list of all titles dumped will appear on the data display and printer output. Dump can be aborted at any time by simply pressing down the pen on the tablet.

The LOAD pictures, write enable a Disc, press LIBRARY, LOAD, PICTURE followed by optional keyword, END. The screen is wiped to black and the system waits for the digital interface to detect a valid input. The green LED will light on the Interface card when the input is OK. The message "Ignoring picture : title" will be given if the title does not contain the keyword. This picture is transferred to framestore but not written to disc. A list of all transfers appears on the data display and printer output. Again one can abort by pressing the pen on the tablet.

4. CHECKING THE DIGITAL INTERFACE SYSTEM

See also Input Locking - Adjustments
Digital Interface - Adjustments

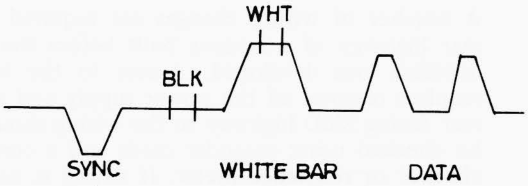
Power on reset of the machine should set the Digital Interface into the idle state and the digital output should be the idle pattern (see circuit description). This output may be fed up the digital input and used to set up the Input Locking card. First check the line sync to white bar timing of the digital output is within specification.

PAL	11.0 – 11.2μs
NTSC	10.6 – 11.0μs

When loading, the Input Locking card separates syncs from the digital input using the same circuitry as for live video so if live video locks then this is probably adjusted correctly. Mixed syncs is generated on TP14 (MS). To check the digital data slicer feed the digital output into the digital input and pull out the Input Timing card. This card drives the source selects which then default to digital input (labelled VTR on circuit diagram).

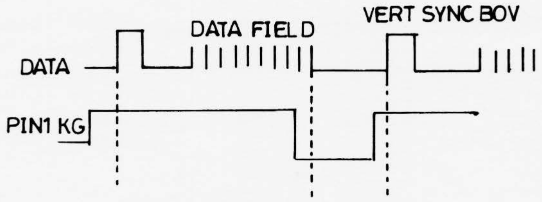
There are four adjustments that may be necessary on the Input Locking card.

(a) Trigger a scope on MS and look at pin 1 of DC (DG 184) at line rate. This is filtered digital data. Check the filter links are in the correct position (PAL or NTSC). The white and black sample pulses cause glitches on this signal so their position can easily be checked. Use the WHT and BLK adjustment pots to position the pulses as below.



(b) Hang scope on DATA test point and adjust slice level ADAT so that black and white data pulses have equal mark space ratio. If the slicer does not appear to work properly move link 4 to F and manually slice using FDAT.

(c) Adjust sample blanking SB so that the white sample pulses are gated off when there are no white bars during field group. Trigger scope off FLD and compare signal on pin 1 of KG with the data on pin 1 of DA.



(d) Check line reset. Adjust LR to give reset pulse at LINE with trailing edge 1-2μs before the white sync bar.